

# LCFC Confidential


## G 320 AST M/B Schematics Document

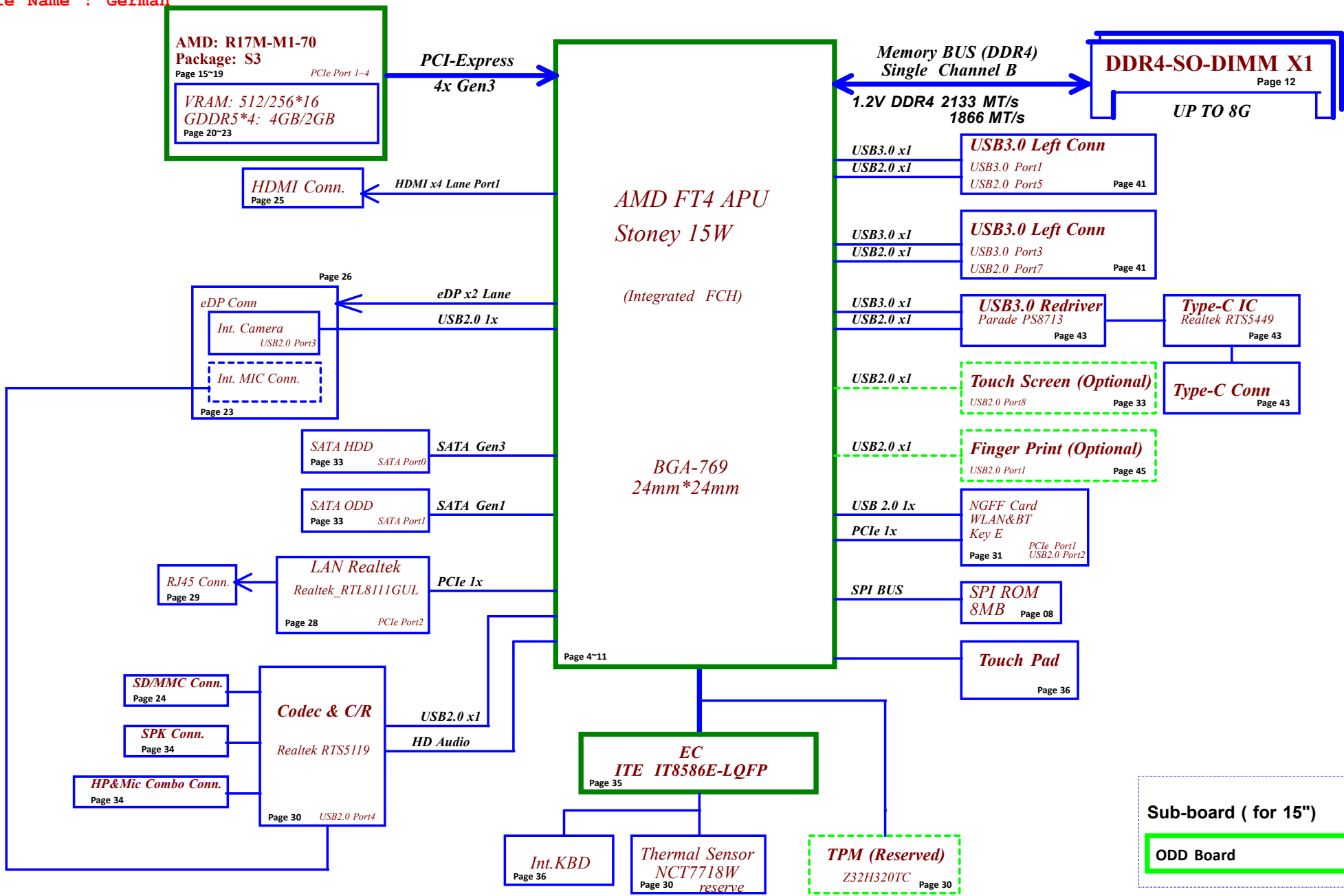
NM\_B321 REV:0.2

AMD FT4 Stoney SOC with DDRIII

AMD R17M-M1-70

2017-02-04

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Issued Date	2017/02/04	Deciphered Date	2017/02/04	<b>Cover Page</b>		
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Sub-board ( for 15")

ODD Board

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## Voltage Rails ( O --&gt; Means ON , X --&gt; Means OFF )

power plane	State	B+ (+20VSB)  +3VL  +5VLP	+5VALW (+3VALW_APU)  +1.8VALW  +0.95VALW  +0.775VALW	+2.5V +1.2V (+VSYSTEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.6VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

BOARD Config.	BOARD_ID1	BOARD_ID2	reserve
	0: Dis	0: No KBL	
	1: UMA	1: KBL	

BOARD Config.	BOARD_ID0	BOARD_ID3
14''	0	0
15''	0	1
17''	1	0

## USB Port Table for Stoney FT4

USB 2.0	USB 3.0	Port	Port device
EHCI		0	Finger print
		1	Blue Tooth
		2	Camera
		3	Card Reader
		4	LEFT USB (3.0)
xHCI	2	5	Type-C
		6	RighT USB (3.0) upper
		7	Touch screen

## PCIE PORT LIST

	Port	Device
GPP	0	N/A
	1	WLAN
	2	LAN
	3	N/A
GFX	0	DIS GPU
	1	
	2	
	3	

## BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_PX@	EMC GPU part
EMC_CZ@	EMC Carrizo APU part
EMC_15@	EMC 15 part
RF_NS@	RF reserve Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
AOAC@	AOAC support part
HDT@	HDT Debug part
TS@	Touch screen part
CZ@	Carrizo Part
CZL@	CarrizoL part
CZPX@	Carrizo Discrete Part
CZLPX@	CarrizoL Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2GX4@	X76 SAMSUNG 1G
M2GX4@	X76 MICRON 1G
H2GX4@	X76 HYNIX 1G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
S1G@	SAMSUNG 1G
M1G@	MICRON 1G
H1G@	HYNIX 1G
CZLUMA@	CarrizoL UMA Part
CZUMA@	Carrizo UMA Part
SIVCD@	SIV COST down material
HDMI@	HDMI Logo
STN@	Stoney part
KBL@	Key board backlight part

## SMBUS Control Table

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	X	V		X	X	X	X	V	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V	X		X	X	V	V APU_SIC APU_SID 1.8VS For APU	X	X	X
APU_SMB_CLK APU_SMB_DATA	APU +3VS	X	X	X	V	V	X		X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VL_EC	X	X		X	X	X	X	X	V	X
TP_I2C0_SCL_R TP_I2C0_SDA_R	APU +1.8VS	X	X	X	X	X	X		X	X	V

## EC SM Bus1 address EC SM Bus2 address EC SM Bus3 address

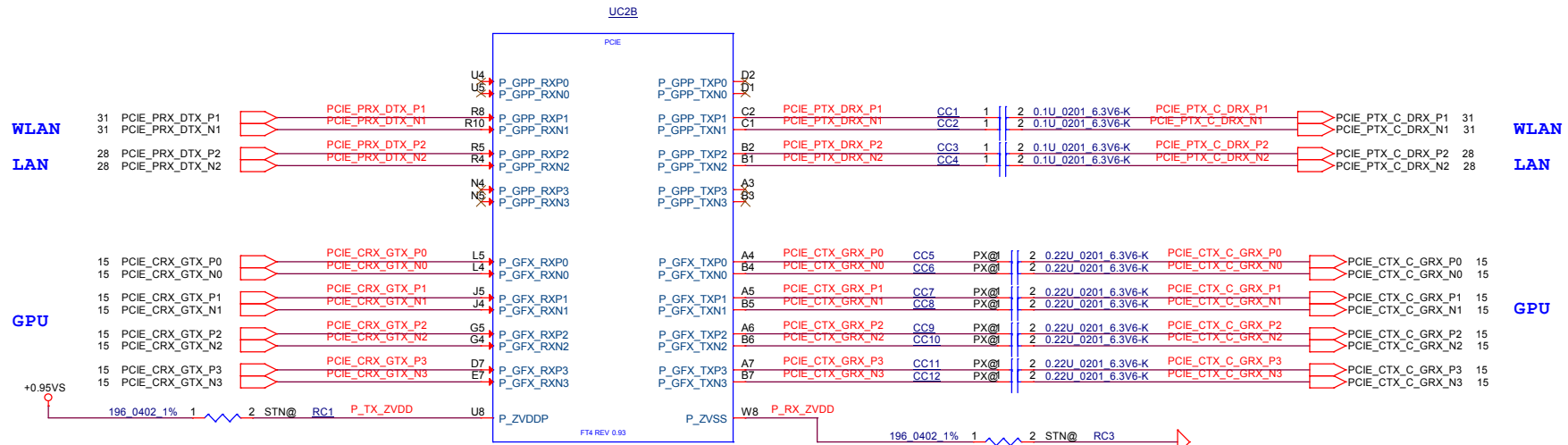
Device	Address	Device	Address	Device	Address
Battery	0X16	PMIC	0X34	Thermal Sensor	1001_100xb(reserve)
Charger	0001 0010 b			GPU	0x41(default)
				APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting

## APU SM Bus1 address APU SM Bus2 APU SM Bus3 address APU SM Bus4

Device	Address	Device	Address
Touch pad	0x15	DDR DIMM	0xA0h
		WLAN	RSVD

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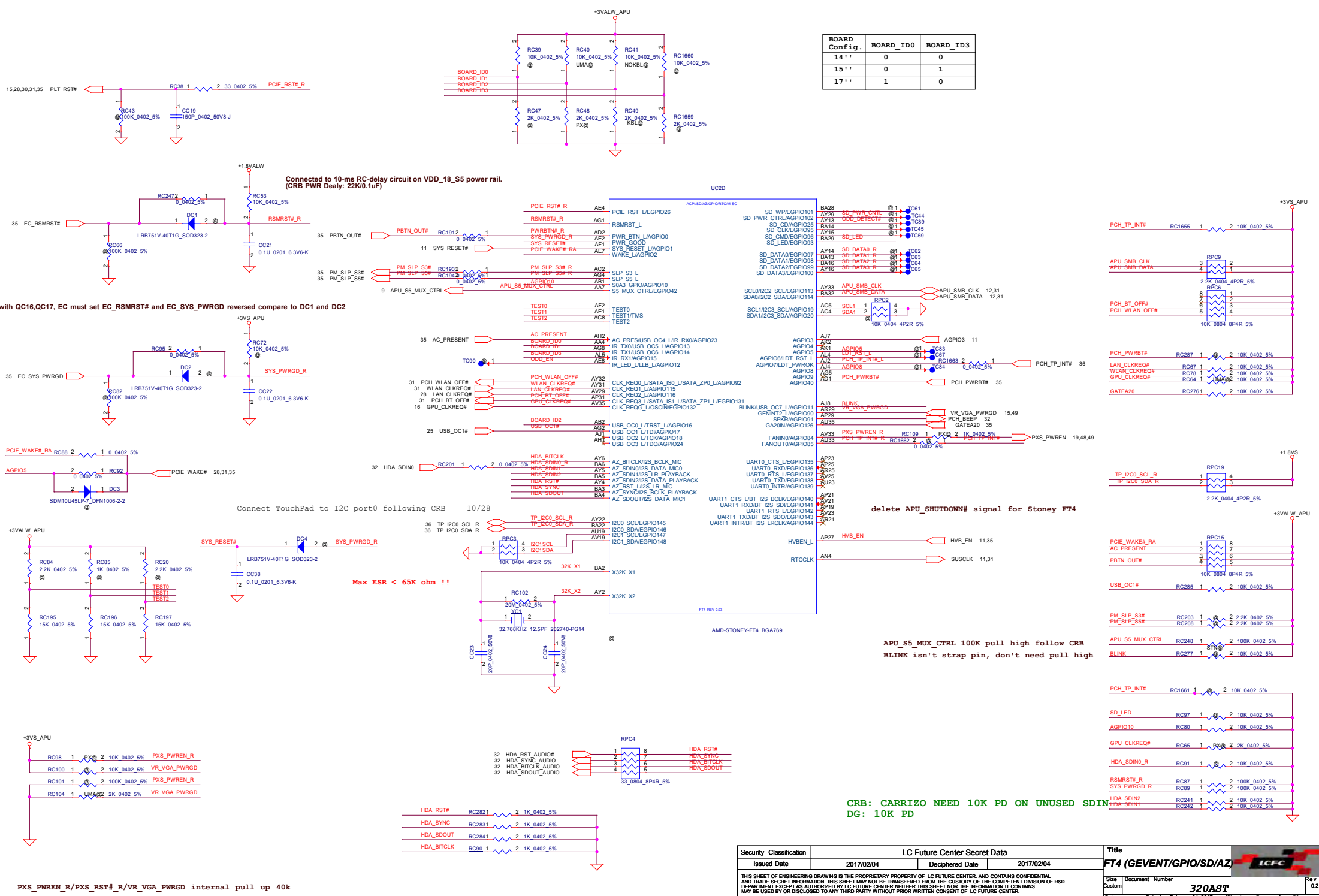


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Issued Date	2017/02/04	Deciphered Date	2017/02/04	FT4 (PCIE I/F)	
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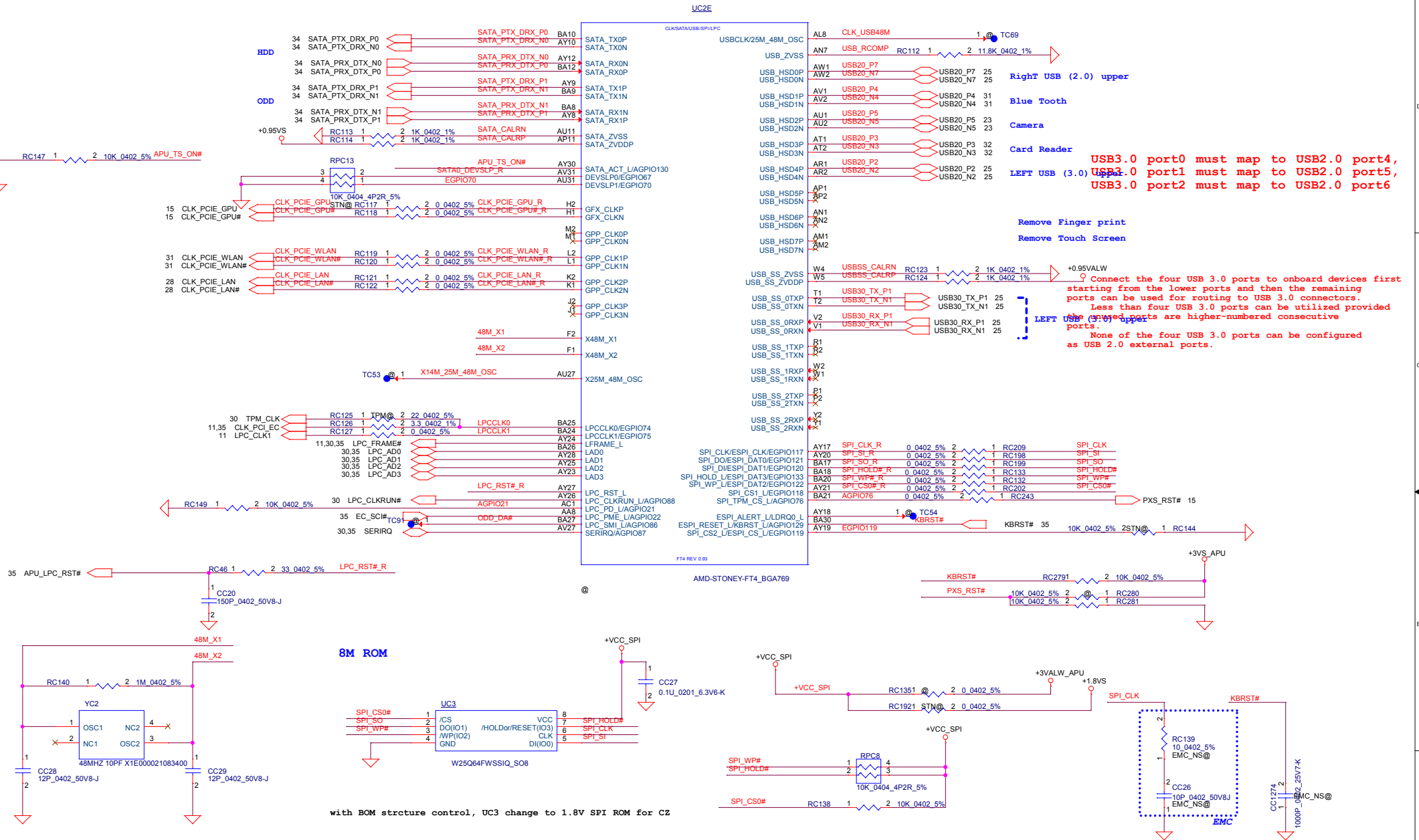




BOARD Config.	BOARD_ID0	BOARD_ID3
14''	0	0
15''	0	1
17''	1	0

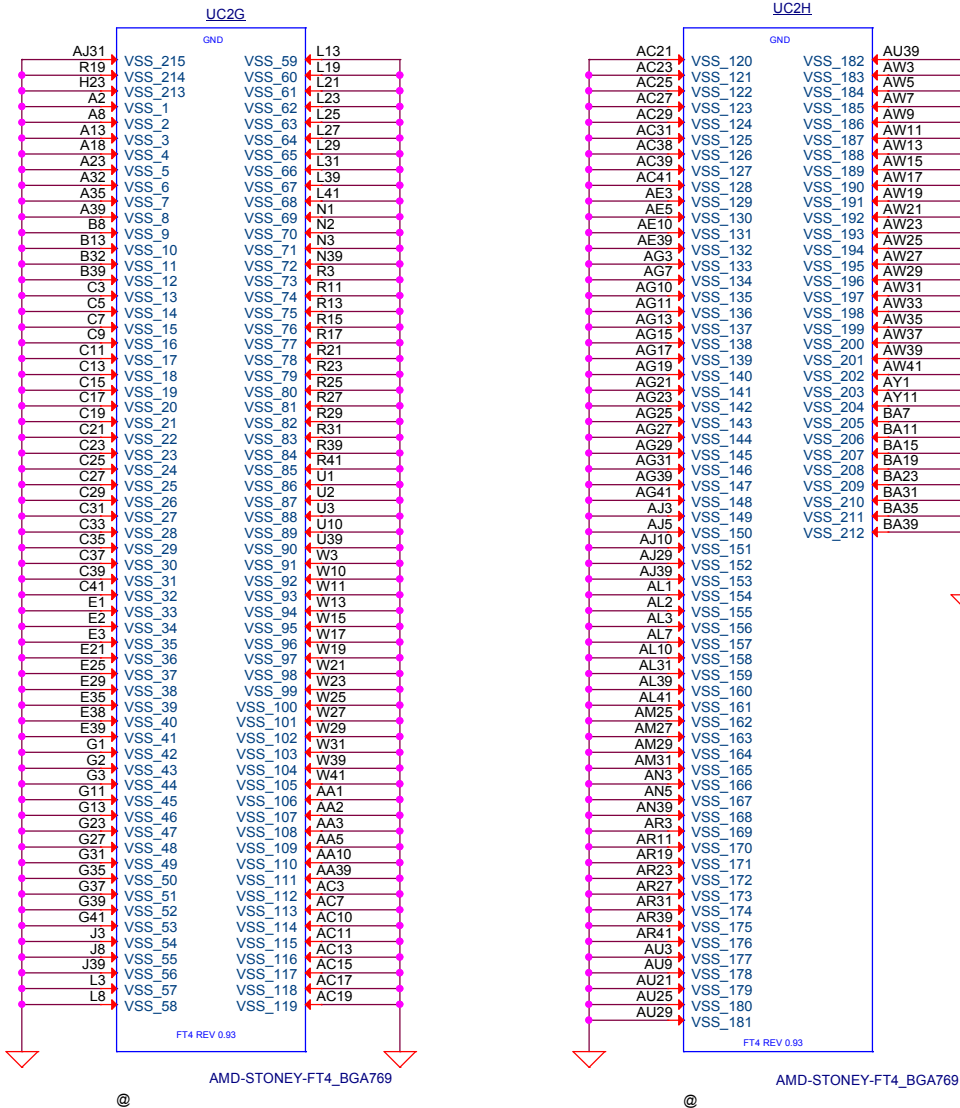
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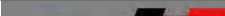






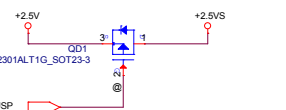
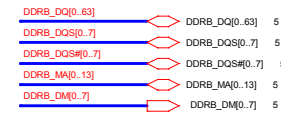
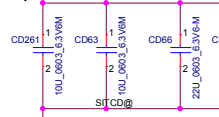
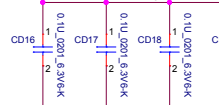
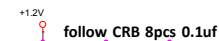
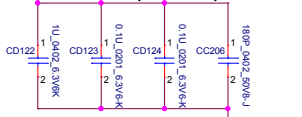
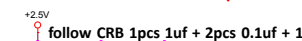
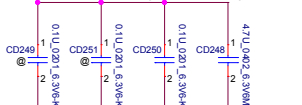
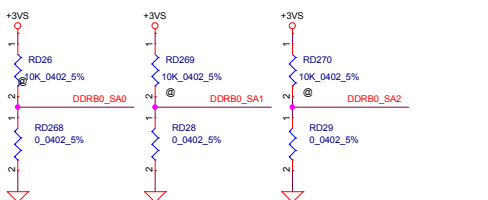
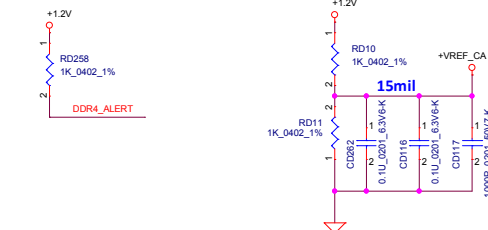
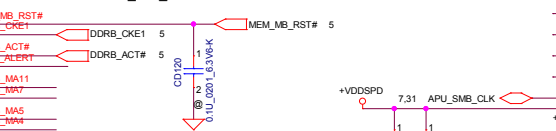
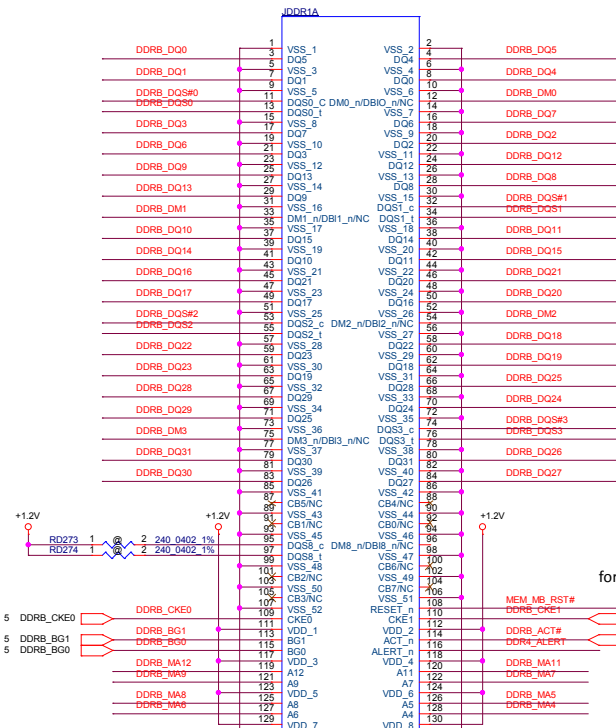




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**DDR4 SO-DIMM A**



CPU Address = A0H

SPD Address = A0H

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## Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.

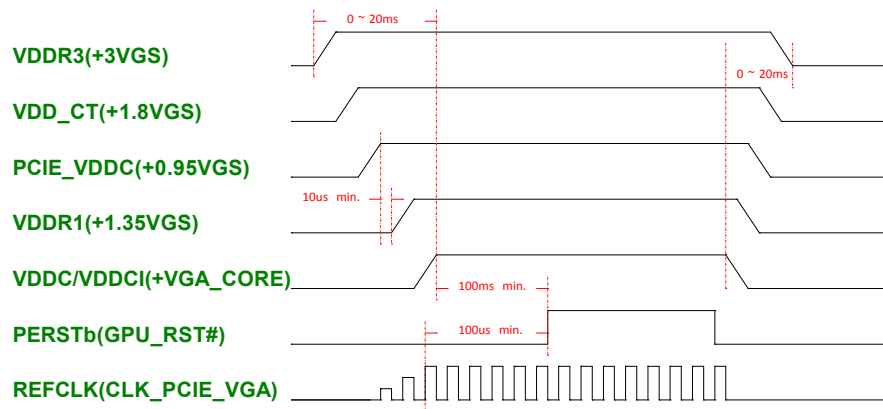
It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10  $\mu$ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU.

The gate circuits must meet the slew rate requirement (such as  $\leq$  50 mV/ $\mu$ s).

For power down, reversing the ramp-up sequence is recommended.



## VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G.N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

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4 PCIe\_CTX\_C\_GRP\_P[0..3] PCIe\_CTX\_C\_GRP\_P[0..3]  
4 PCIe\_CTX\_C\_GRP\_N[0..3] PCIe\_CTX\_C\_GRP\_N[0..3]

PCIE\_CRX\_GTX\_P[0..3] PCIe\_CRX\_GTX\_P[0..3] 4  
PCIE\_CRX\_GTX\_N[0..3] PCIe\_CRX\_GTX\_N[0..3] 4

PCIE\_CTX\_C\_GRP\_P0 AF30  
PCIE\_CTX\_C\_GRP\_N0 AE31

UV1A

PCIE\_RX0P  
PCIE\_RX0N

PCIE\_TX0P  
PCIE\_TX0N

AH30 PCIE\_CRX\_C\_GRP\_P0 0.22U 0201 6.3V6-K 1 2 PX@ CV1 PCIE\_CRX\_GTX\_P0  
AG31 PCIE\_CRX\_C\_GRP\_N0 0.22U 0201 6.3V6-K 1 2 PX@ CV2 PCIE\_CRX\_GTX\_N0

PCIE\_CTX\_C\_GRP\_P1 AE29  
PCIE\_CTX\_C\_GRP\_N1 AD28

PCIE\_RX1P  
PCIE\_RX1N

PCIE\_TX1P  
PCIE\_TX1N

AG29 PCIE\_CRX\_C\_GRP\_P1 0.22U 0201 6.3V6-K 1 2 PX@ CV3 PCIE\_CRX\_GTX\_P1  
AF28 PCIE\_CRX\_C\_GRP\_N1 0.22U 0201 6.3V6-K 1 2 PX@ CV4 PCIE\_CRX\_GTX\_N1

PCIE\_CTX\_C\_GRP\_P2 AD30  
PCIE\_CTX\_C\_GRP\_N2 AC31

PCIE\_RX2P  
PCIE\_RX2N

PCIE\_TX2P  
PCIE\_TX2N

AF27 PCIE\_CRX\_C\_GRP\_P2 0.22U 0201 6.3V6-K 1 2 PX@ CV5 PCIE\_CRX\_GTX\_P2  
AF26 PCIE\_CRX\_C\_GRP\_N2 0.22U 0201 6.3V6-K 1 2 PX@ CV6 PCIE\_CRX\_GTX\_N2

PCIE\_CTX\_C\_GRP\_P3 AC29  
PCIE\_CTX\_C\_GRP\_N3 AB28

PCIE\_RX3P  
PCIE\_RX3N

PCIE\_TX3P  
PCIE\_TX3N

AD27 PCIE\_CRX\_C\_GRP\_P3 0.22U 0201 6.3V6-K 1 2 PX@ CV7 PCIE\_CRX\_GTX\_P3  
AD26 PCIE\_CRX\_C\_GRP\_N3 0.22U 0201 6.3V6-K 1 2 PX@ CV8 PCIE\_CRX\_GTX\_N3

AB30  
AA31

PCIE\_TX4P  
PCIE\_TX4N

AC25  
AB25

AA29  
Y28

PCIE\_TX5P  
PCIE\_TX5N

Y23  
Y24

Y30  
W31

PCIE\_TX6P  
PCIE\_TX6N

AB27  
AB26

W29  
V28

PCIE\_TX7P  
PCIE\_TX7N

Y27  
Y26

V30  
U31

NC#V30  
NC#U31

W24  
W23

U29  
T28

NC#U29  
NC#T28

V27  
U26

T30  
R31

NC#T30  
NC#R31

U24  
U23

R29  
P28

NC#R29  
NC#P28

T26  
T27

P30  
N31

NC#P30  
NC#N31

T24  
T23

N29  
M28

NC#N29  
NC#M28

P27  
P26

M30  
L31

NC#M30  
NC#L31

P24  
P23

L29  
K30

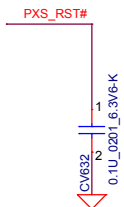
NC#L29  
NC#K30

M27  
M26

PCI EXPRESS INTERFACE

with BOM strcture control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD(EXO-S3 PRO), symbol check ok  
11/4 change to PC sample SA000074V10



8 CLK\_PCIE\_GPU CLK\_PCIE\_GPU# AK30  
8 CLK\_PCIE\_GPU# CLK\_PCIE\_GPU# AK32

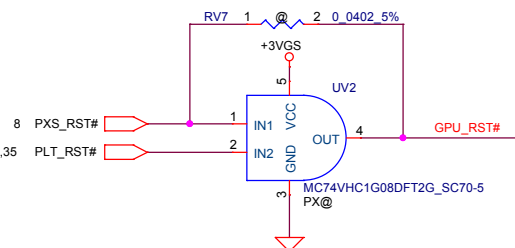
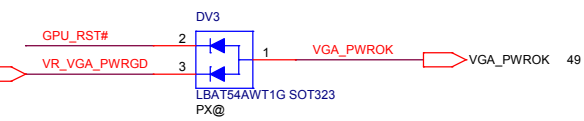
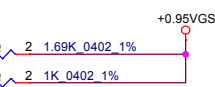
CLOCK  
PCIE\_REFCLKP  
PCIE\_REFCLKN

1K 0402 1% 1 PX@ 2 RV4 N10  
16 GPU\_RST# GPU\_RST# AL27

TEST\_PG  
PERSTB

CALIBRATION

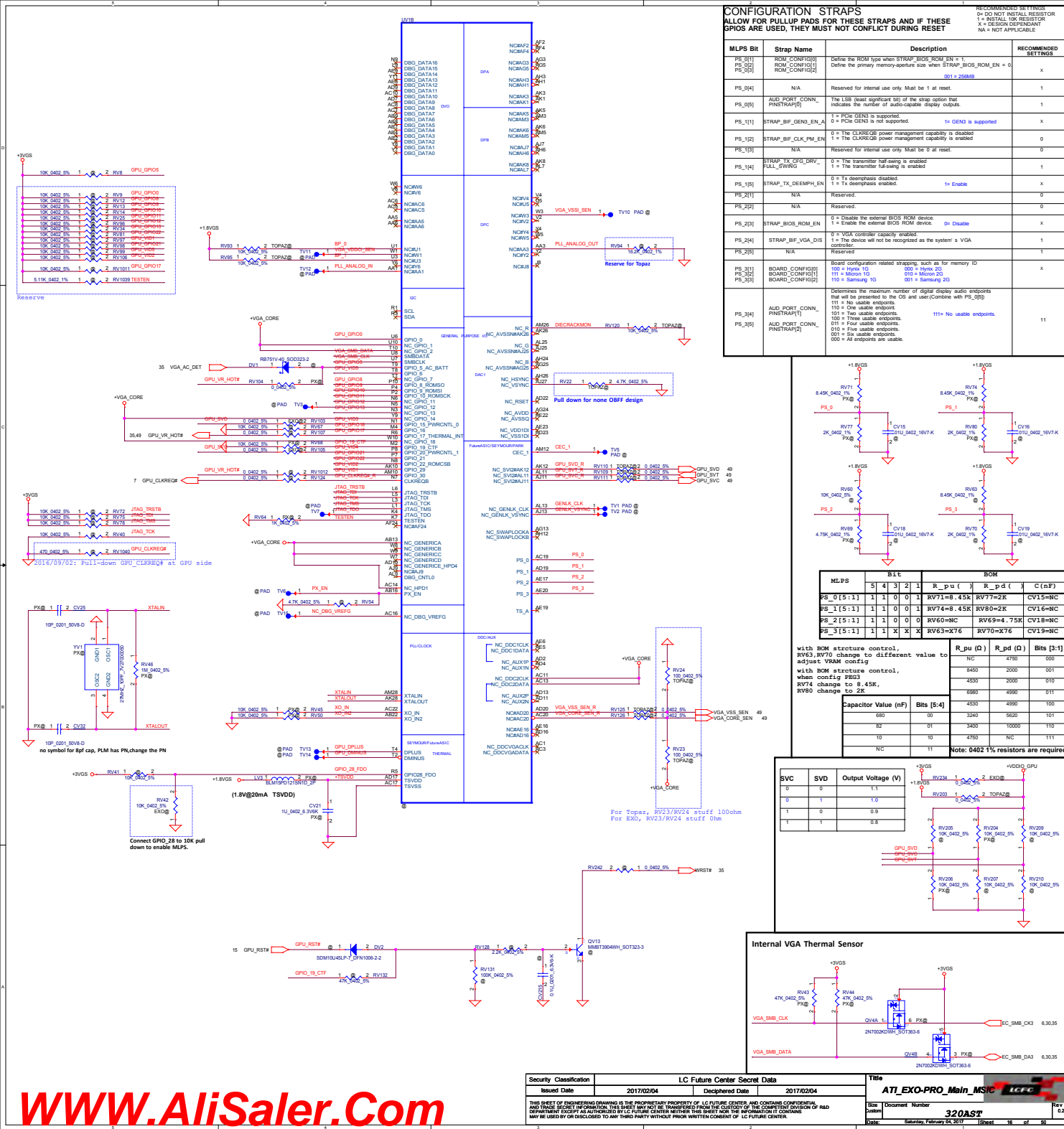
PCIE\_CALR\_TX  
PCIE\_CALR\_RX



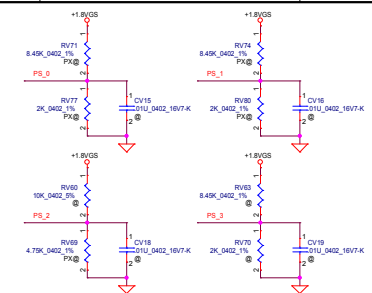
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ATI_EXO-PRO_PCIE		Rev 0.2	
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CONFIGURATION STRAPS				RECOMMENDED SETTINGS
ALLOW FOR PULLUP STRAP FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET				DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR 0 = DESIGN DEPENDANT NA = NOT APPLICABLE
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS	
PS_0[1]	ROM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	x	
PS_0[2]	ROM_CONFIG[1]	Define the primary memory aperture size when STRAP_BIOS_ROM_EN = 0	001 = 256MB	
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1	
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1	
PS_1[1]	STRAP_BIF_GENK_EN_A	0 = PCIe GEN2 is supported 1 = PCIe GEN2 is not supported	1 = GEN2 is supported	
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ power management capability is disabled 1 = The CLKREQ power management capability is enabled	0	
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0	
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = transmitter full-swing is enabled 1 = The transmitter full-swing is disabled	1	
PS_1[8]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled 1 = Tx deemphasis enabled	1 = Enable	
PS_1[11]	N/A	Reserved.	0	
PS_1[12]	N/A	Reserved.	0	
PS_1[13]	STRAP_BIOS_ROM_EN	0 = Enable the external BIOS ROM device 1 = Enable the external BIOS ROM device	0 = Disable	
PS_1[14]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled 1 = The device will not be recognized as the system's VGA controller.	1	
PS_1[15]	N/A	Reserved.	1	
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strap, such as for memory ID	x	
PS_3[2]	BOARD_CONFIG[1]	00 = Hynix 1G 01 = Hynix 2G 10 = Micron 1G 11 = Samsung 1G	00 = Hynix 2G	
PS_3[3]	BOARD_CONFIG[2]	Determines the maximum number of digital display audio endpoints that are presented to the OS and used (Combine with PS_0[5])	111 = No usable endpoints 110 = One usable endpoint 101 = Two usable endpoints 100 = Three usable endpoints 011 = Four usable endpoints 010 = Five usable endpoints 001 = Six usable endpoints 000 = All endpoints are usable.	
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	111 = No usable endpoints 110 = One usable endpoint 101 = Two usable endpoints 100 = Three usable endpoints 011 = Four usable endpoints 010 = Five usable endpoints 001 = Six usable endpoints 000 = All endpoints are usable.	111 = No usable endpoints	
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]		11	



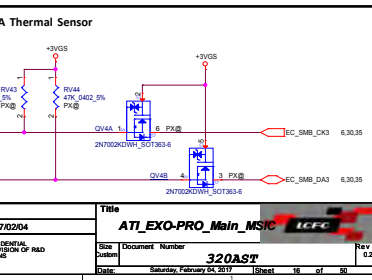
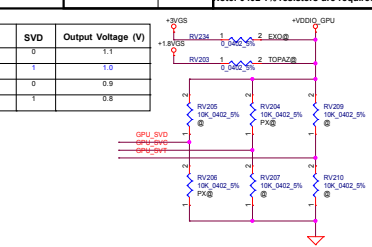
MLPS		Bit				BOM			
		5	4	3	2	R_pu (Ω)	R_pd (Ω)	C(nF)	
PS_0[5:1]	1	1	0	0	0	RV71=8.45K	RV77=2K	CV15=NC	
PS_1[5:1]	1	1	0	0	0	RV74=8.45K	RV80=2K	CV16=NC	
PS_2[5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC	
PS_3[5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=NC	

with BOM structure control, RV63, RV70 change to different value to adjust VDRAM config

with BOM structure control, when config PEG3, RV74 change to 8.45K, RV80 change to 2K

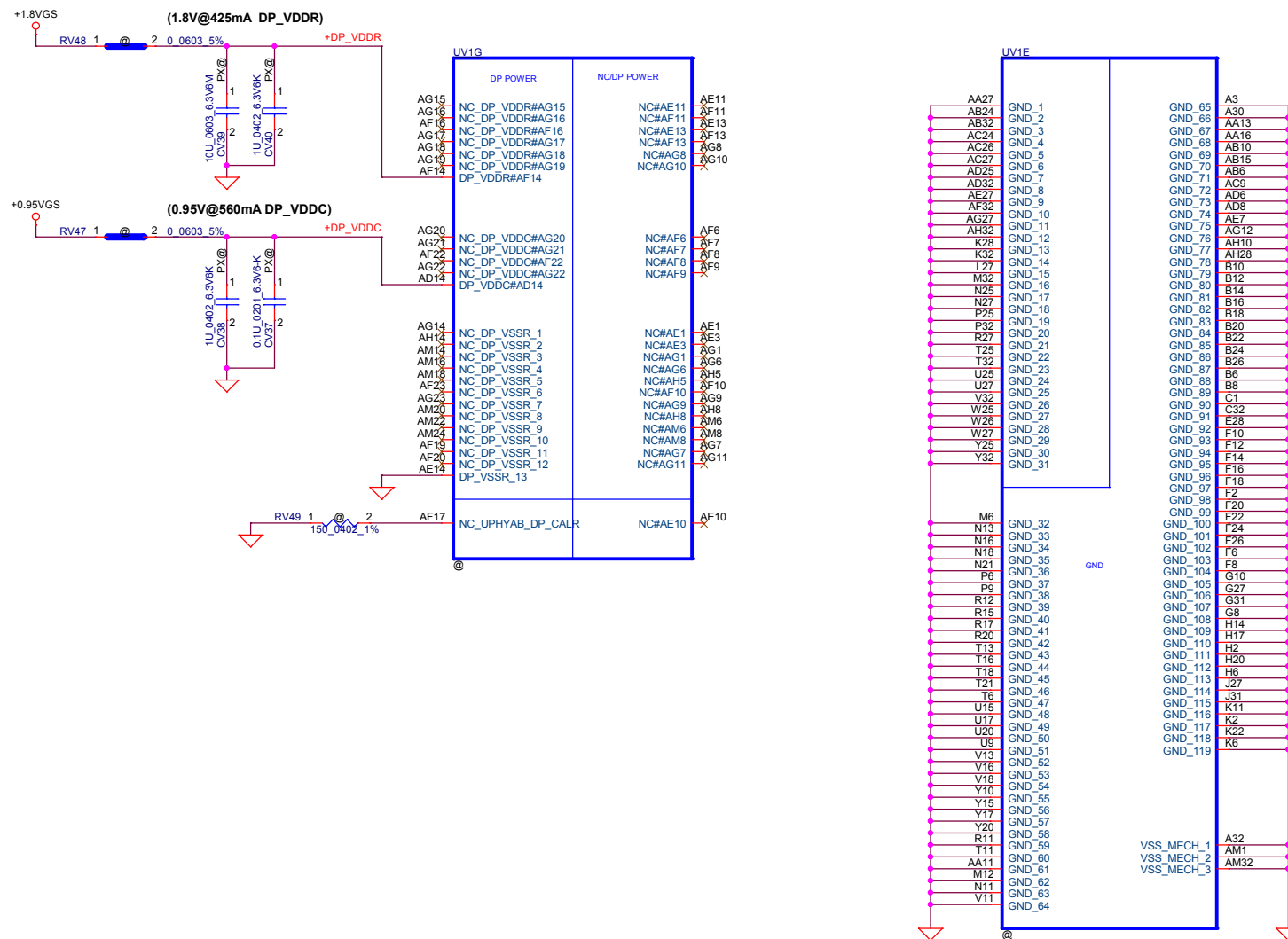
Capacitor Value (nF)	Bits (5:4)
680	00
82	01
10	10
NC	11

Note: 0402 1% resistors are required

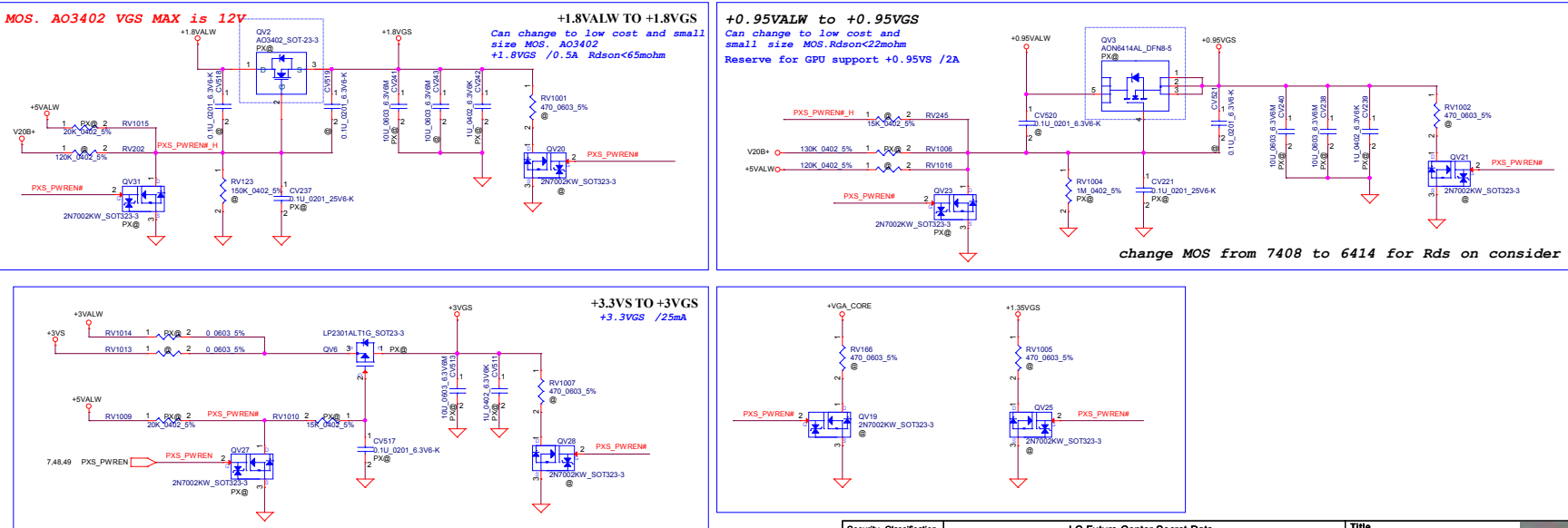




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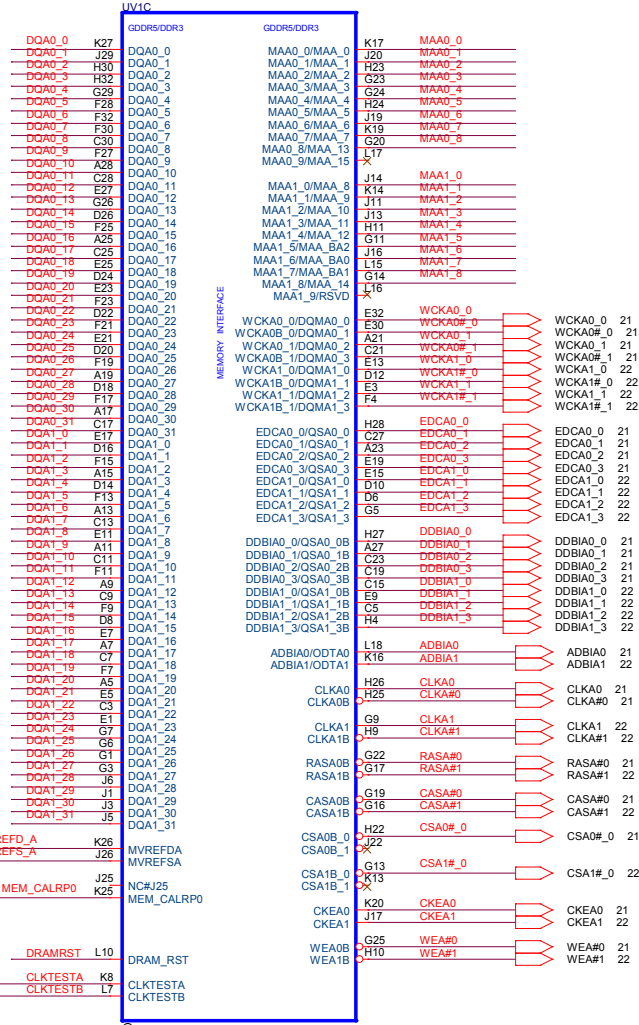
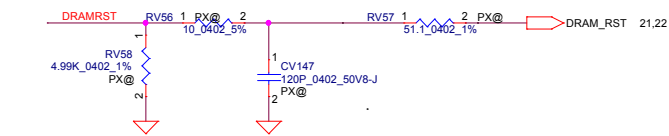
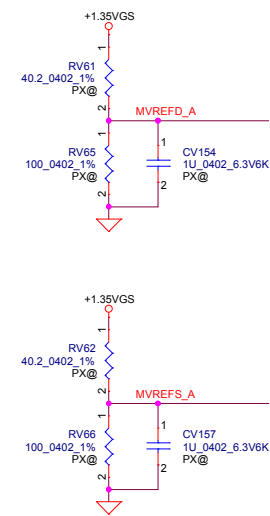
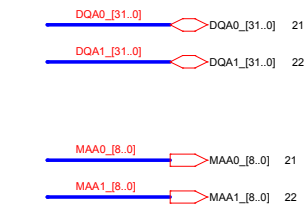
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Size Custom	Document Number	<b>320AST</b>	
Date:	Saturday, February 04, 2017	Sheet	19 of 50
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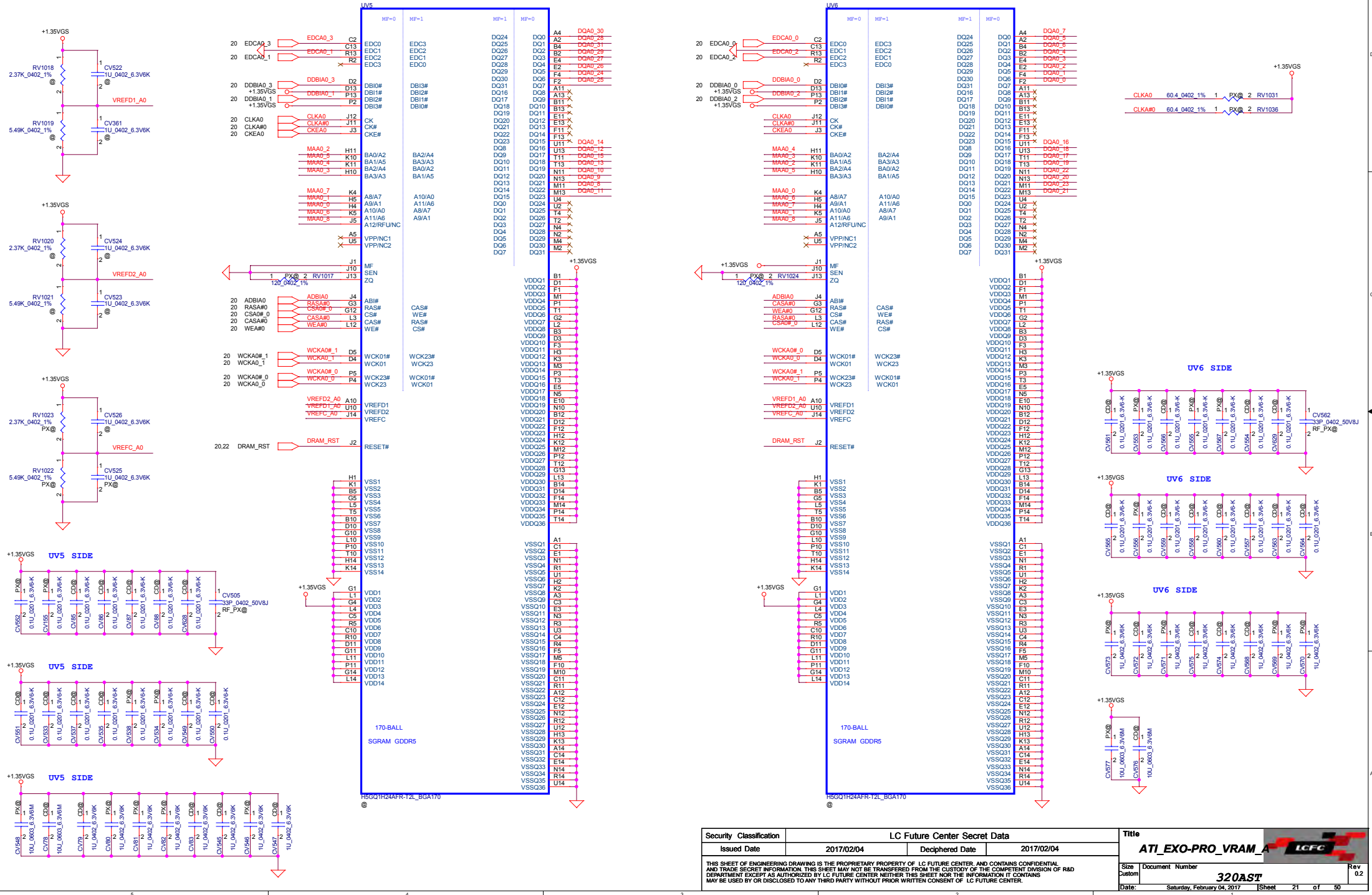
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2017/02/04	Deciphered Date	2017/02/04	ATI_EXO-PRO_MEM IF	
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# Lower 32 bits



## MF=0 No Mirror

## MF=1 Mirror



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Title	AT1_EXO-PRO_VRAM_A		
Size	Document Number	320AST	
Date:	Saturday, February 04, 2017	Sheet	21 of 50

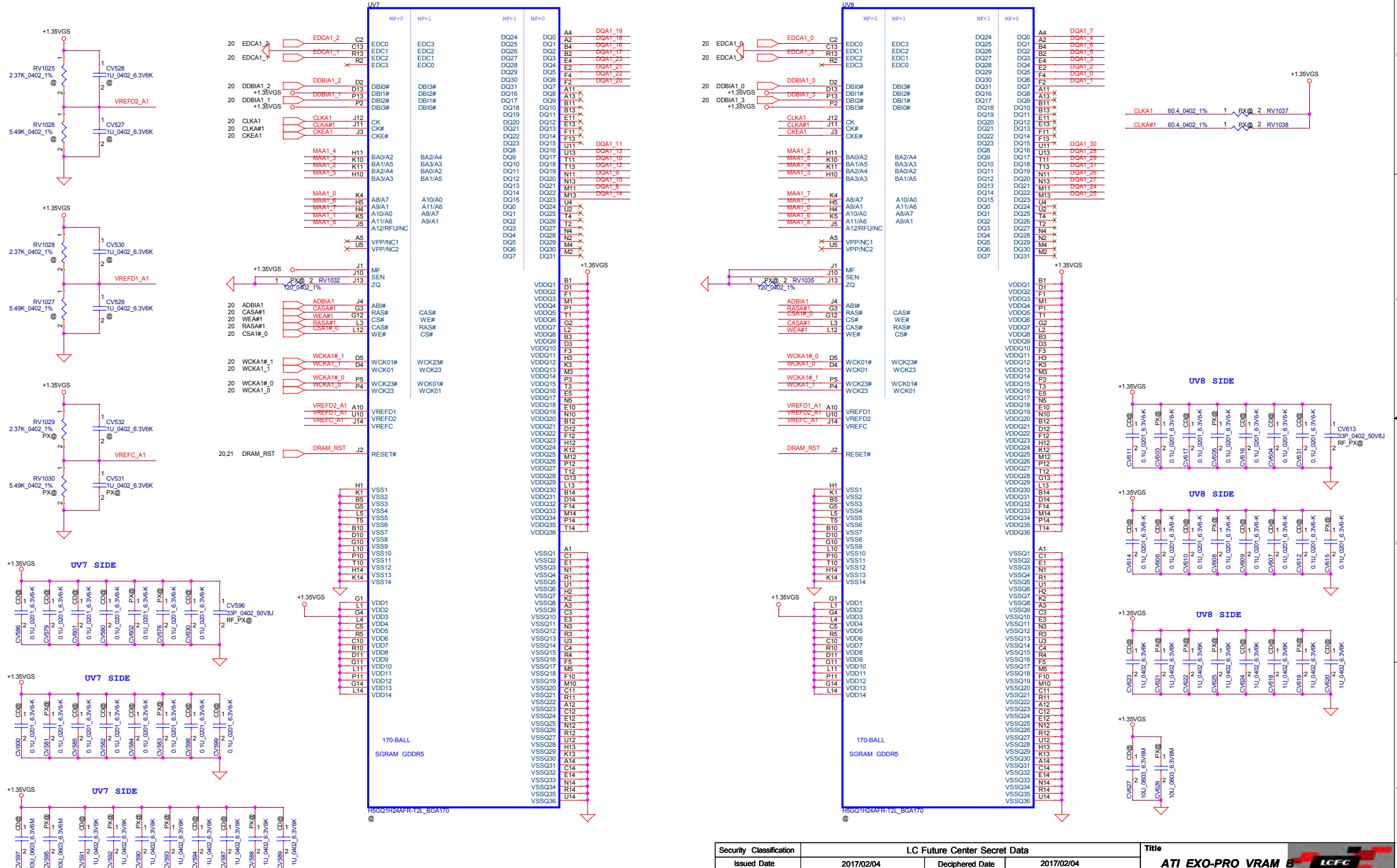


# Upper 32 bits

DQA1\_[31..0] 20  
MAA1\_[8..0] 20

## MF=1 Mirror


## MF=0 No Mirror

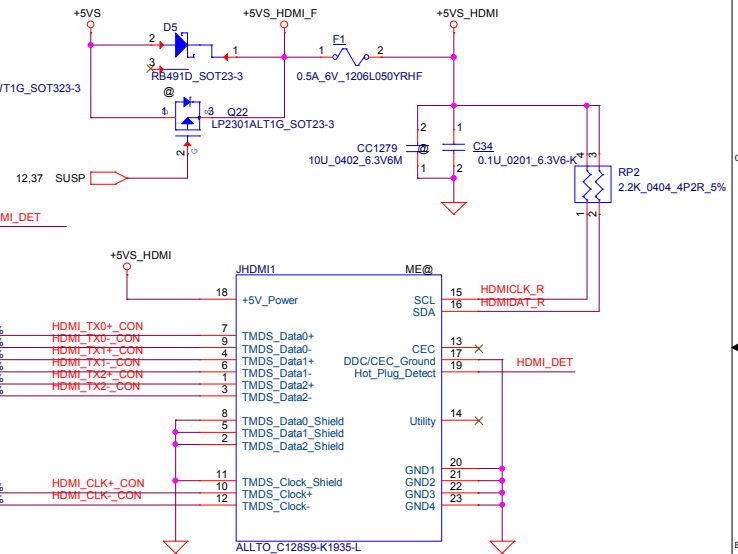
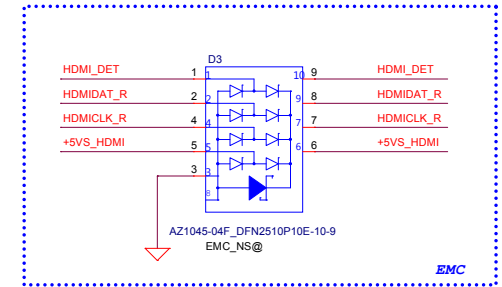
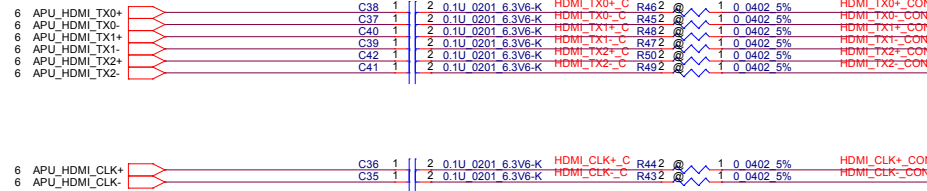
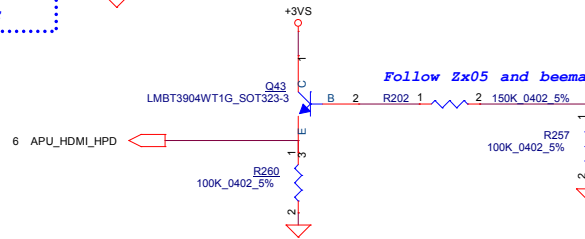
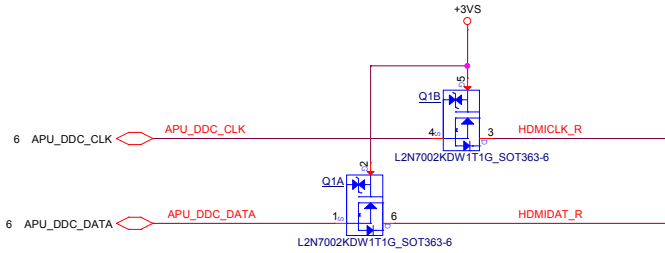
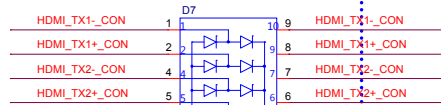
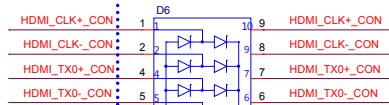
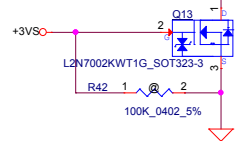
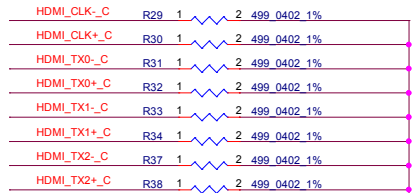
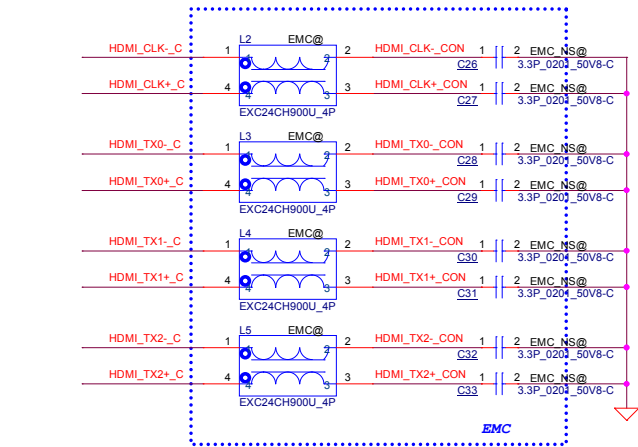




[illegible]

## Remove Touch screen for 320 AST

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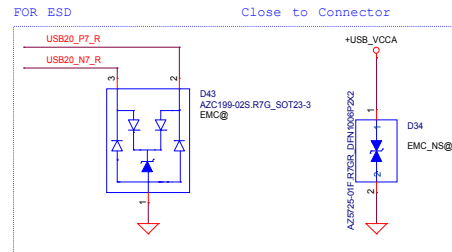
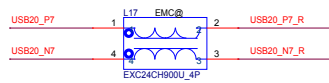
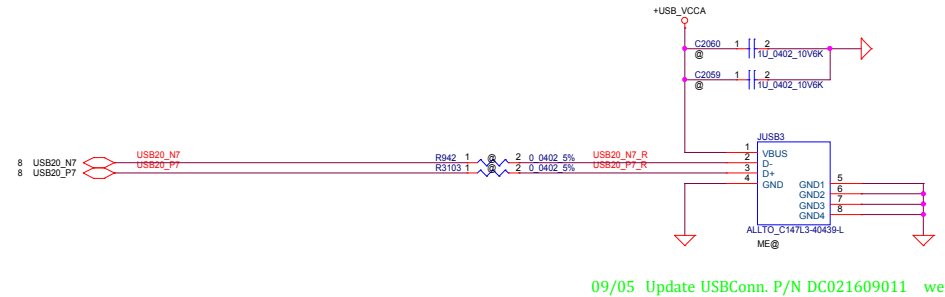
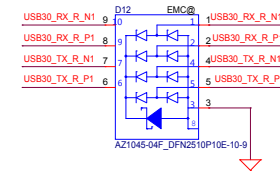
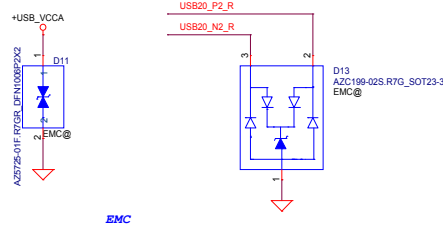
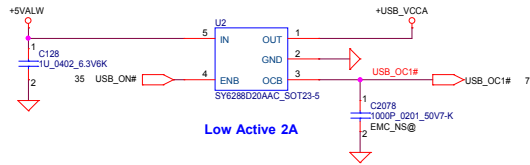
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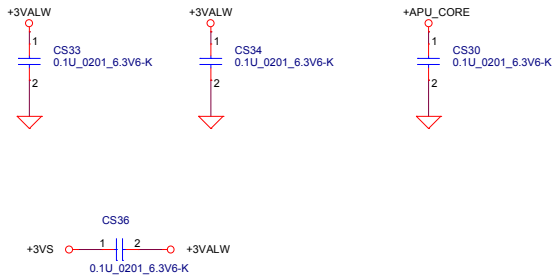
Timing diagram for USB30 signals. The diagram shows three waveforms: USB30\_RX\_N1, USB30\_RX\_P1, and USB30\_TX\_C\_N1. Each waveform is a differential signal with a period of 100ns. The diagram is labeled L13 EMC@ and EXC24CH900U\_4P.



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Remove USB Type-C follow OD

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2017/02/04		2017/02/04			
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A3		320AST		0.2	
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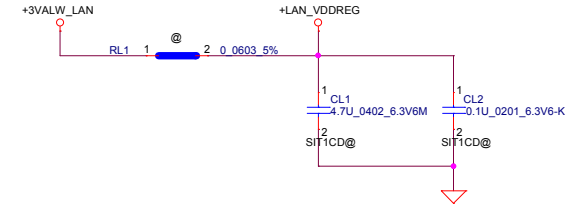


# +3VALW TO +3VALW\_LAN

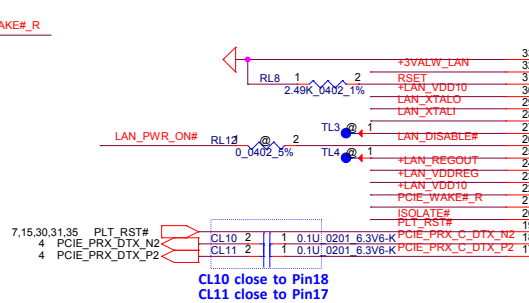
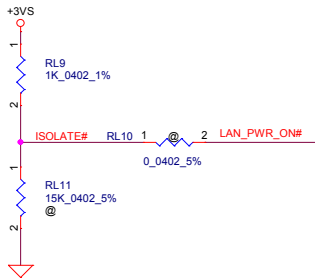
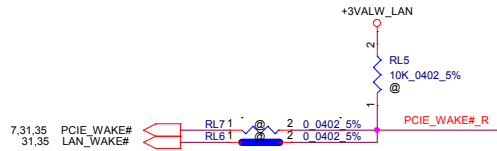
+3VALW\_LAN rising time (10%~90%)  
0.5ms < spec < 10 0m s

Need short

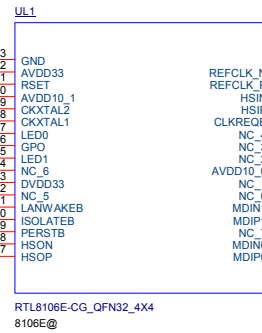
width : 40 mils



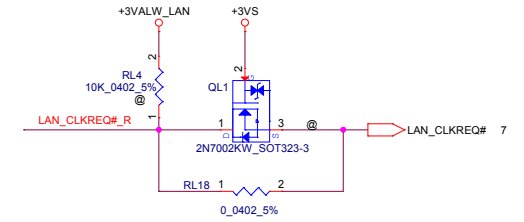
Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32



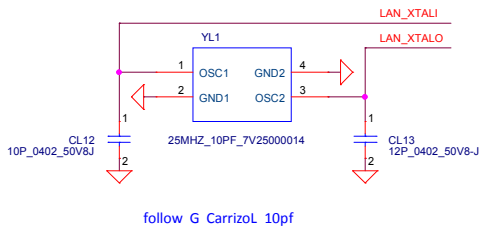
CL10 close to Pin18  
CL11 close to Pin17



RTL8106E-CG\_QFN32\_4X4  
8106E@

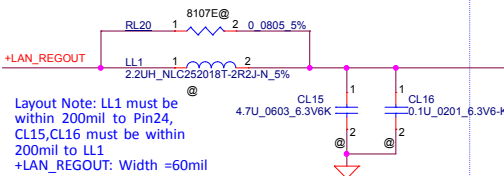


APU CLKREQ all both 3VS power plane

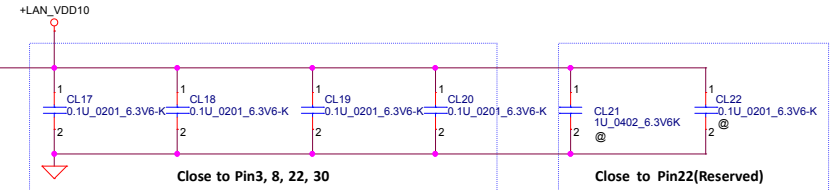


follow G Carrizol 10pf

For RTL8111GUL/ RTL8106EUL (SWR mode)  
For RTL8111H (LDO mode) RL19 stuff



Layout Note: LL1 must be within 200mil to Pin24,  
CL15,CL16 must be within 200mil to LL1  
+LAN\_REGOUT: Width =60mil



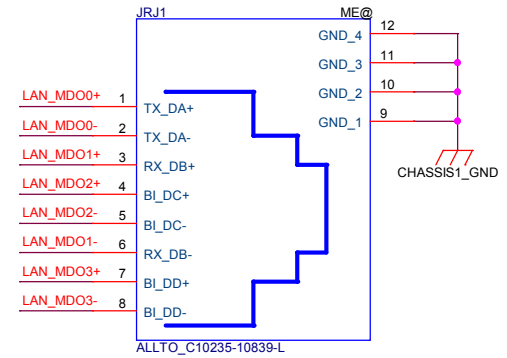
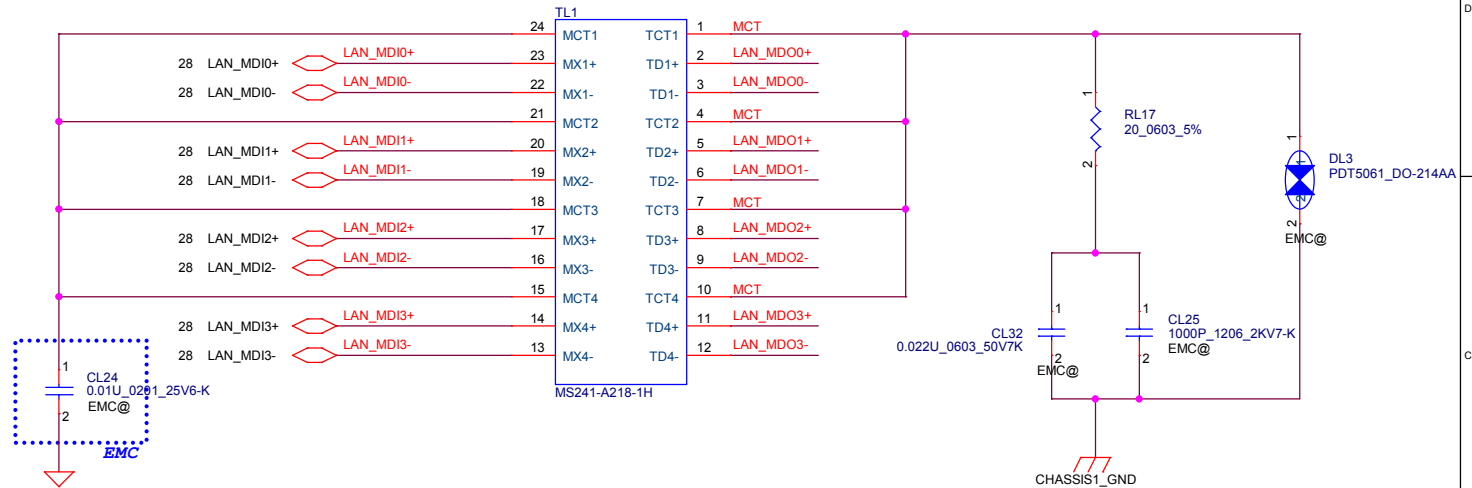
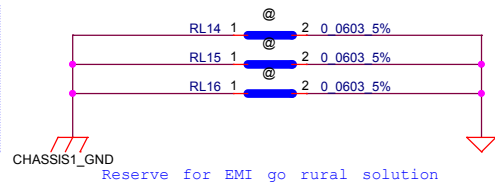
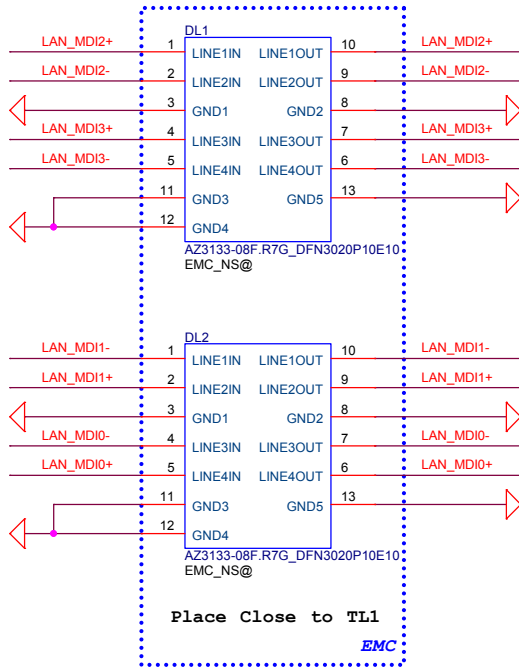
Close to Pin3, 8, 22, 30


Close to Pin22(Reserved)

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2017/02/04		2017/02/04		LAN_RTL8111GUL	
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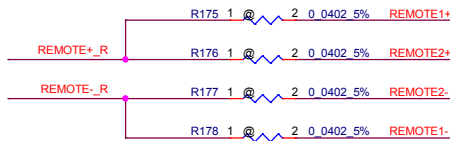
# DL1/DL2 1'S PN:SC300003M00



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										Date:	Saturday, February 04, 2017	Sheet	29	of	50

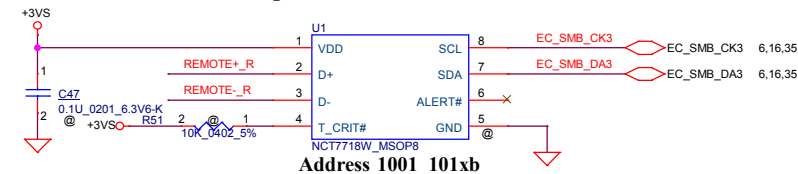


# Close to U1

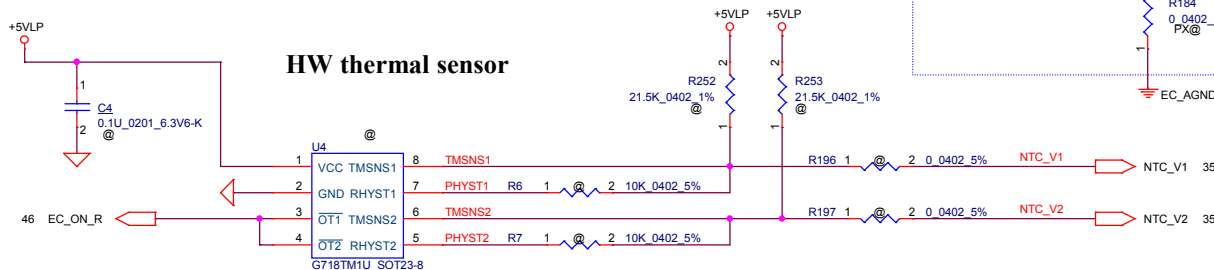


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

# SMSC thermal sensor placed near DIMM



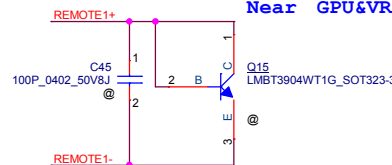
# HW thermal sensor



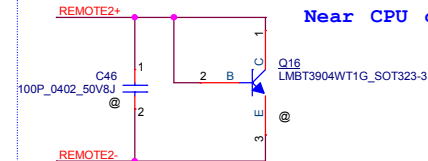
over temperature threshold:  
RSET=3\*RTMH  
92+/-30C  
Hysteresis temperature threshold.  
RHYST=(RSET\*RTML)/(3\*RTML-RSET)  
56+/-30C

	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

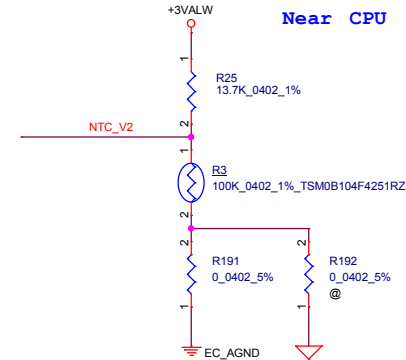
# Near GPU&VRAM



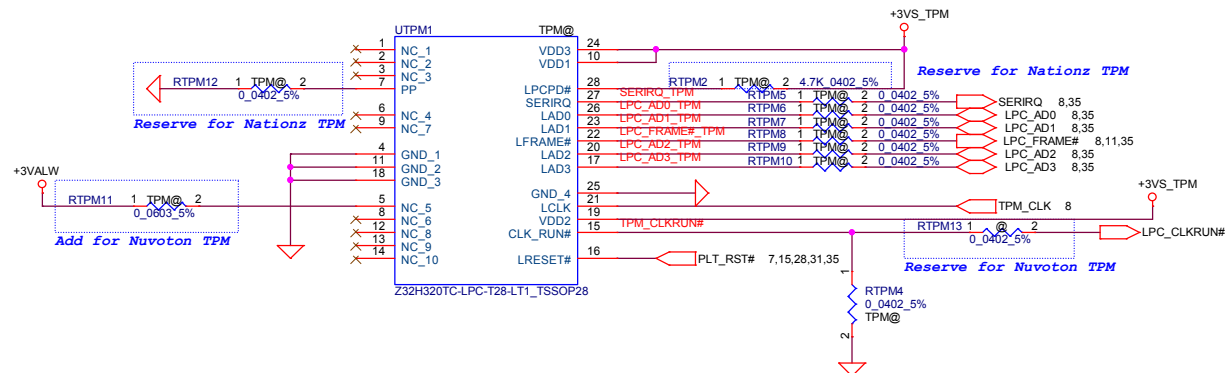
# Near CPU core



# Near CPU



# TPM



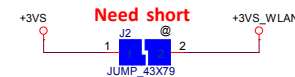
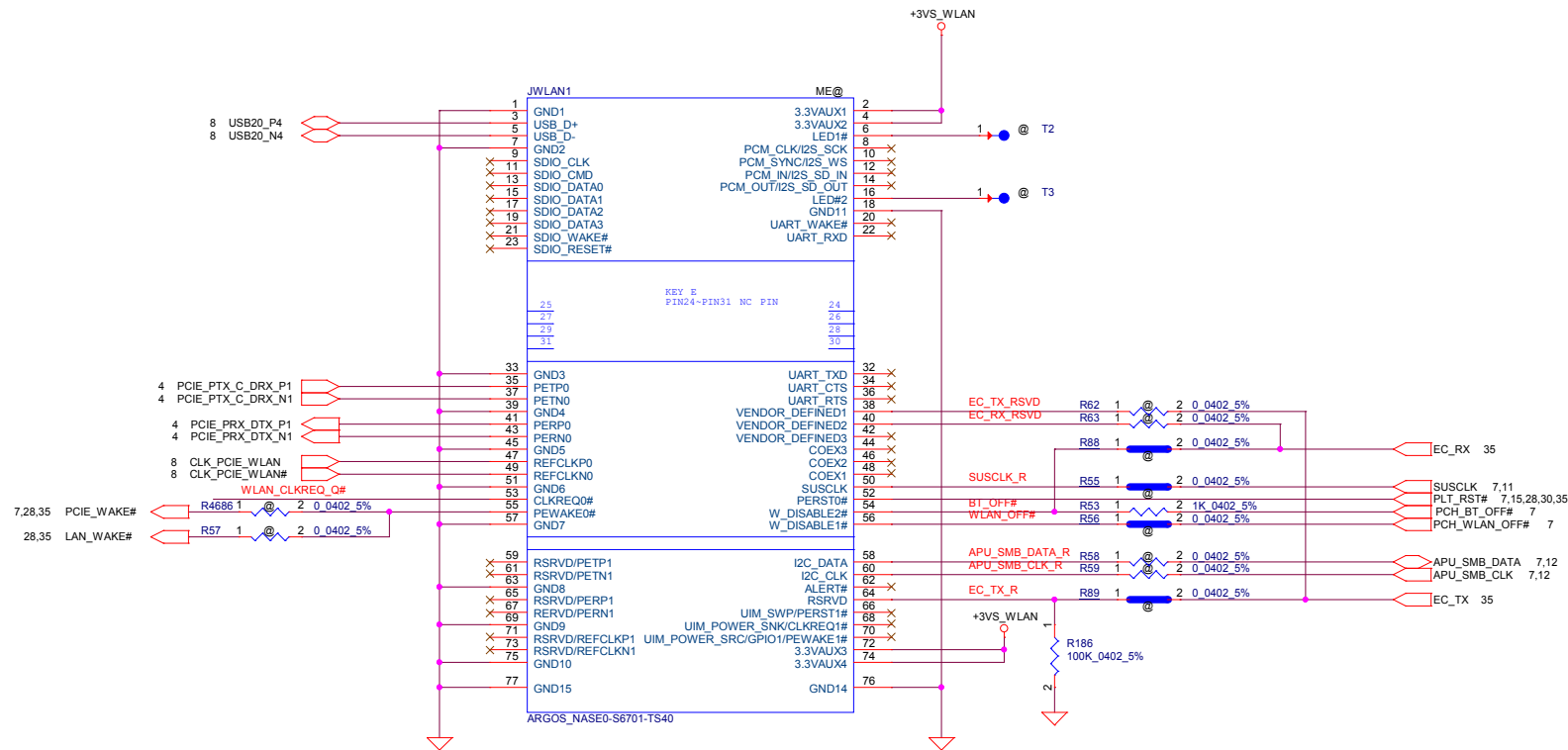
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Title	Thermal sensor/FAN CONN/TPM
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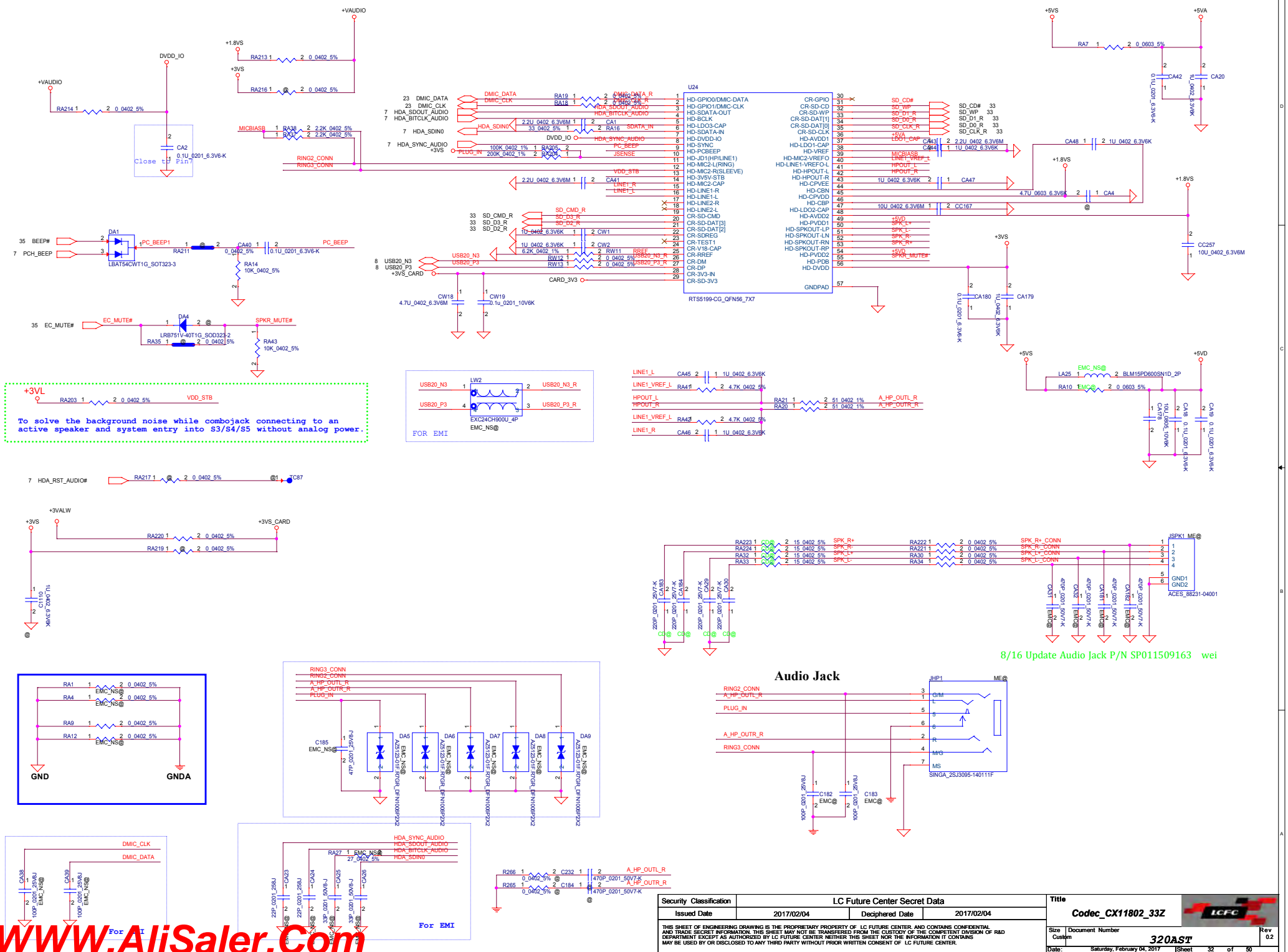
### *Mini-Express Card(WLAN/WiMAX)*

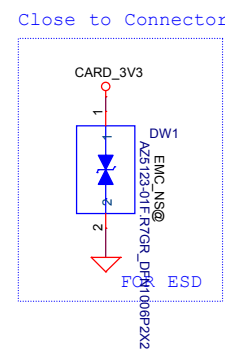
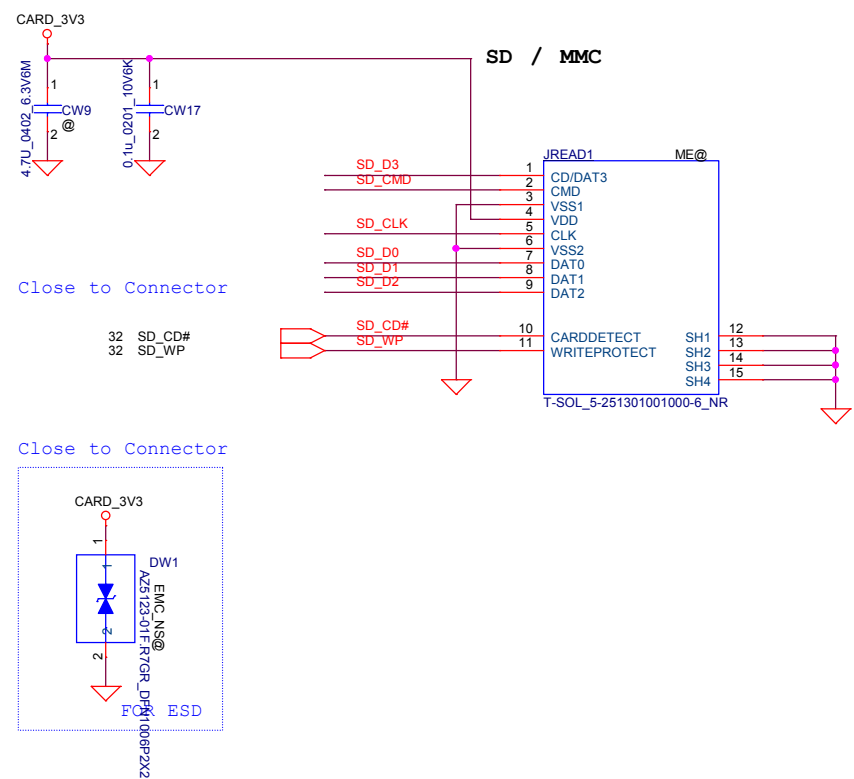
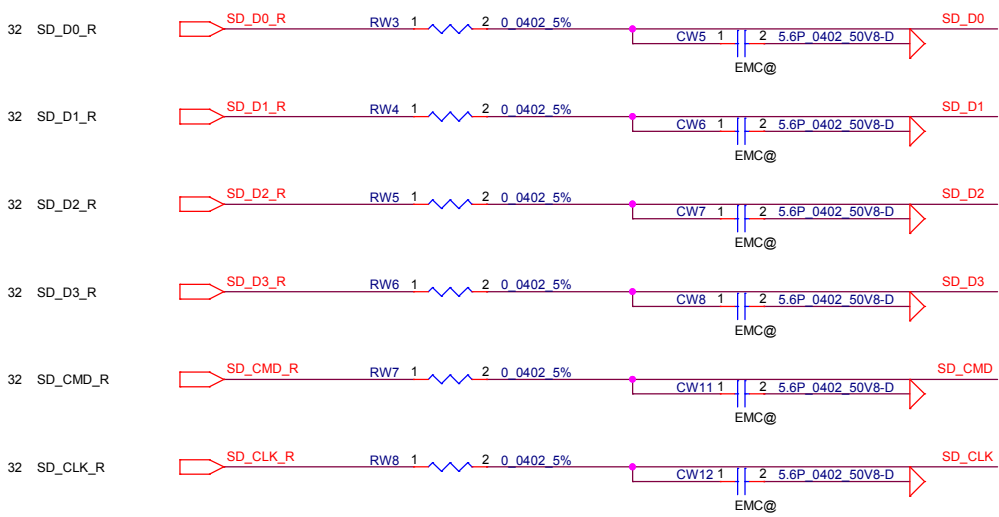



```
If support AOAC, NC R61;
if not support AOAC, stuff R61.
```

Not support AOAC, delete AOAC power circuit 1015

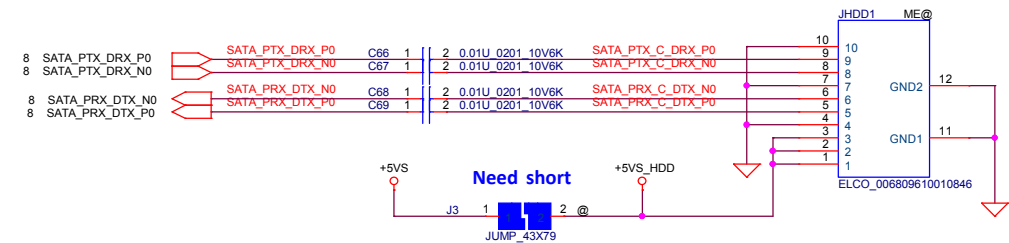
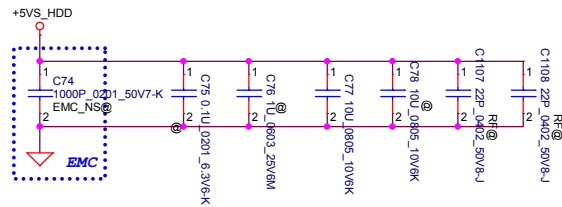
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						Custom		320AST	0.2
						Date:	Saturday, February 04, 2017		Sheet 31 of 50



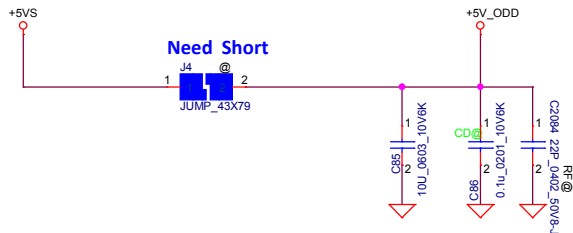


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				Date:	Saturday, February 04, 2017	Sheet 33 of 50	

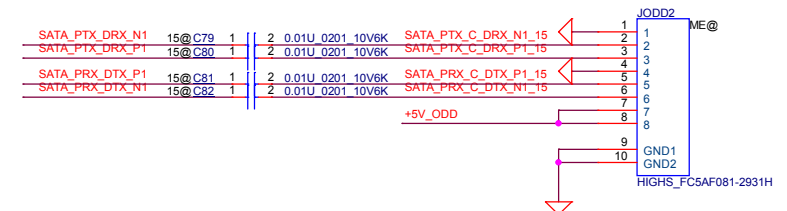
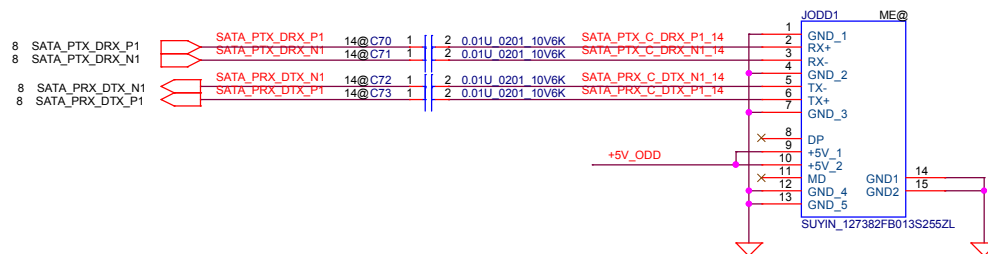
## SATA HDD Conn.




## SATA 15 ODD P/N pin assign is different from G SKL



## FOR 14" SATA ODD Conn.

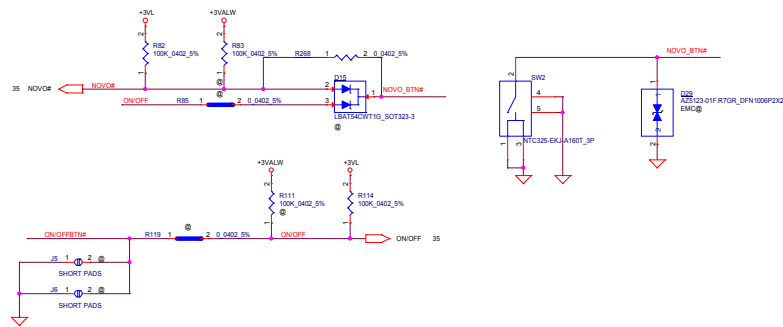


8/16 Update Conn. P/N SP01001YV00 wei

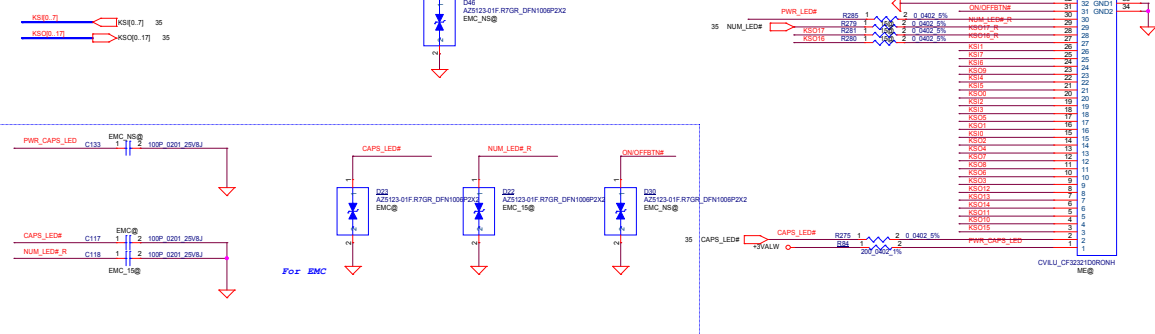
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Issued Date	2017/02/04	Deciphered Date	2017/02/04	HDD/ODD CONN				
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						Custom		
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## ON/OFF switch



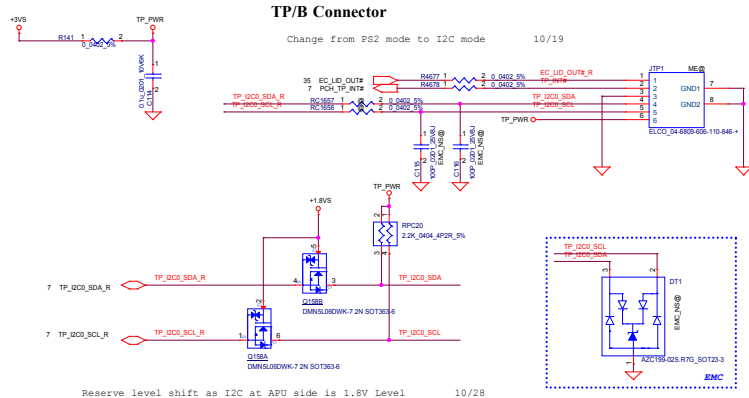
## K/B Connector



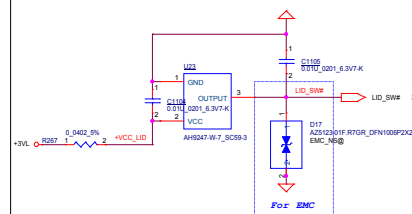
## TP/B Connector

Change from PS2 mode to I2C mode

10/19

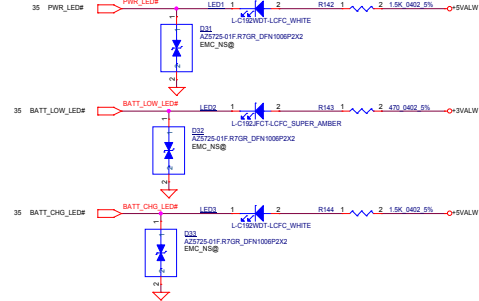


## LID Connector

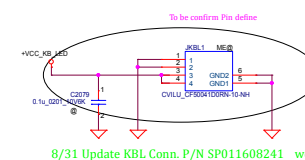
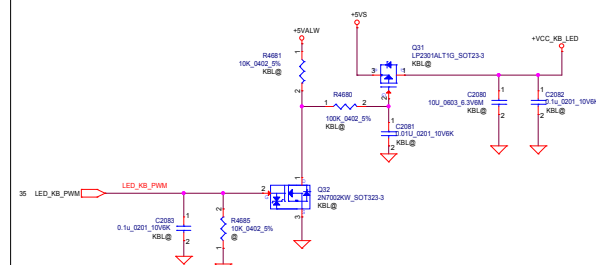


## Finger Print Connector

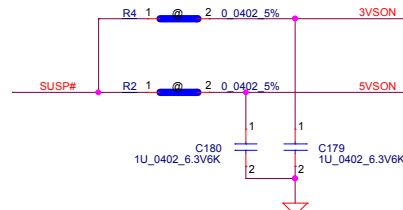
## LED



## KB Backlight Connector



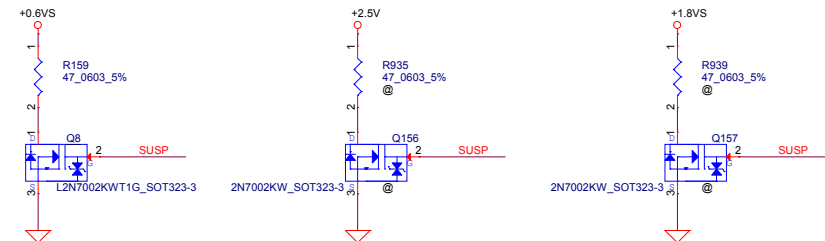
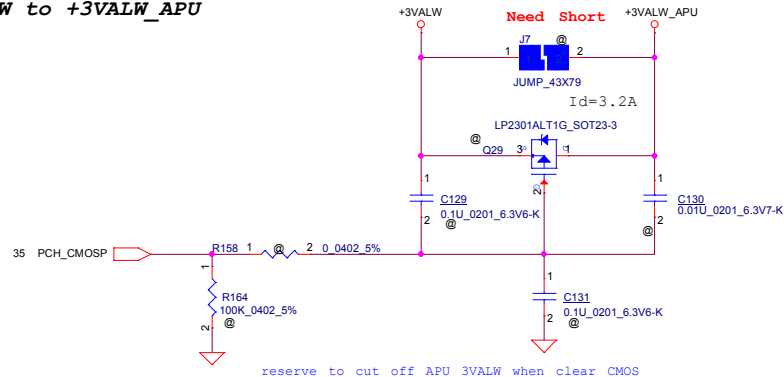
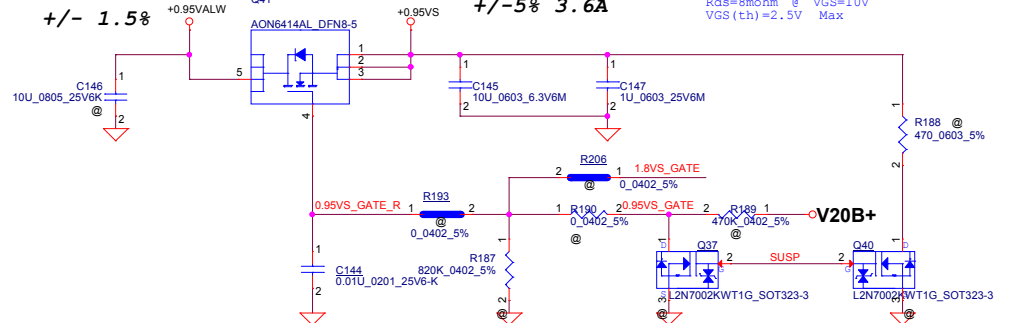
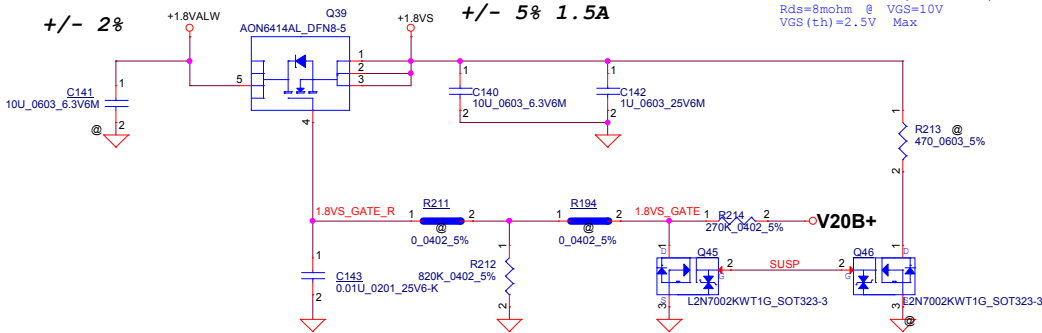
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2017/02/04	Deciphered Date	2017/02/04	KBD/PWR/IO/LED/TP Conn.	
Size	Document Number	320AST		Rev	0.2
Comp	Doc	320AST		Date	February 14, 2017
		Sheet	35	of	89




**SA000067600 (GMT) 7/16**

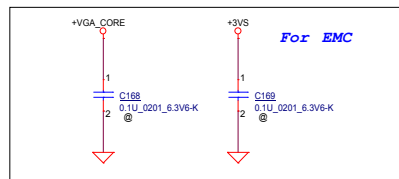
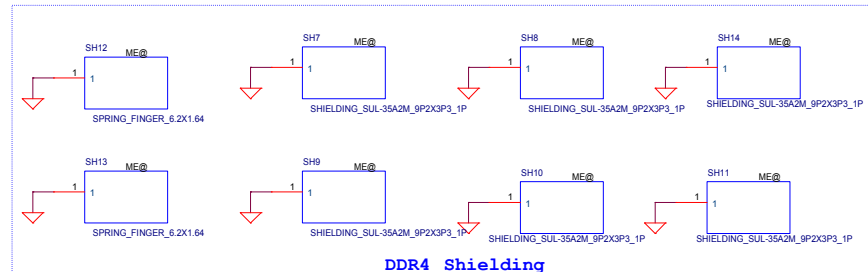
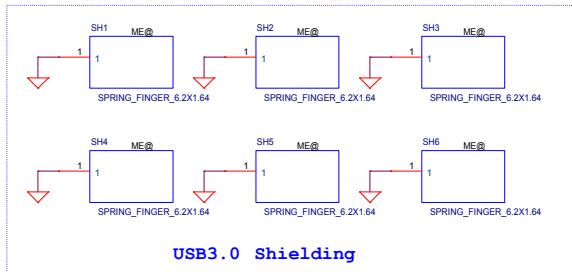
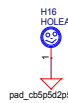
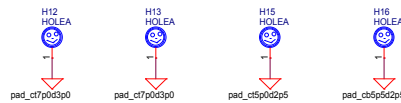
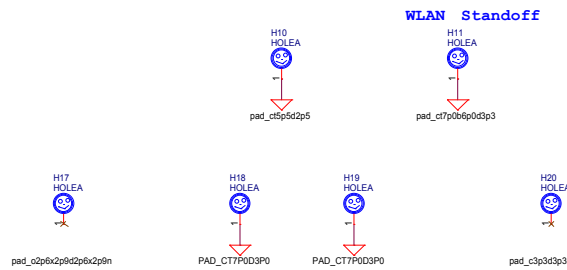
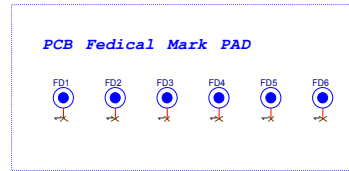
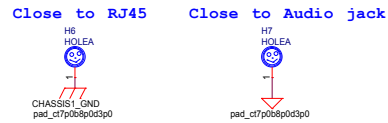
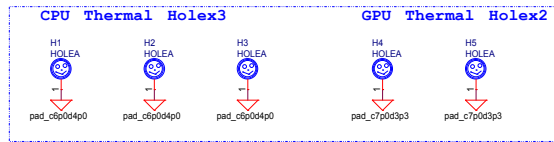
**Need Short**


**Change the main source to SA000067600 (GMT) 7/16**

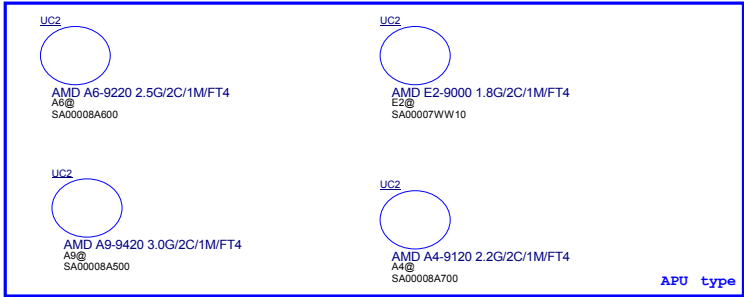
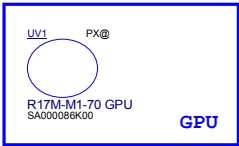
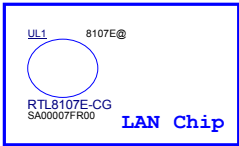


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								Document Number <b>320AST</b>		Rev 0.2
Date: Saturday, February 04, 2017								Sheet 37 of 50		

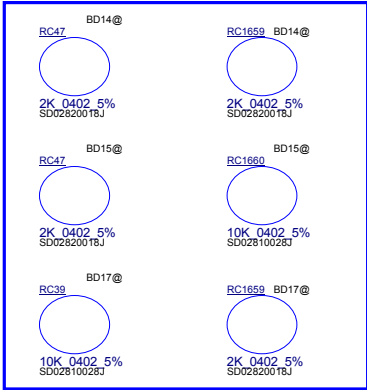




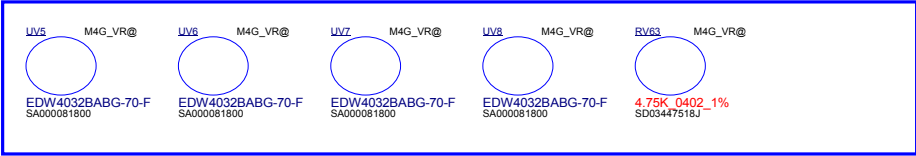
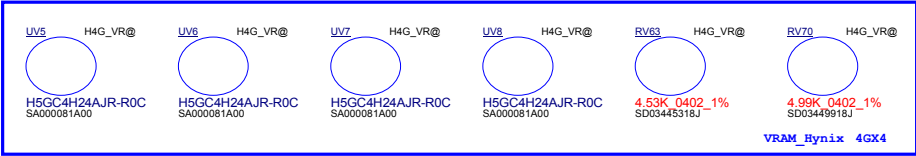
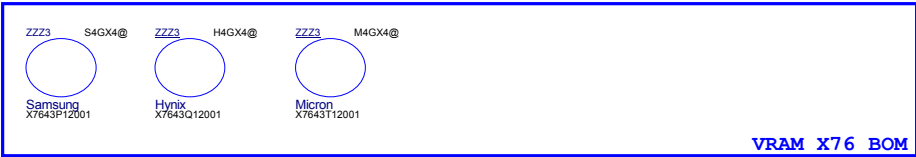
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Issued Date	2017/02/04	Deciphered Date	2017/02/04	Size		
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					320AST	02
Date: Saturday, February 04, 2017					Sheet	38 of 50

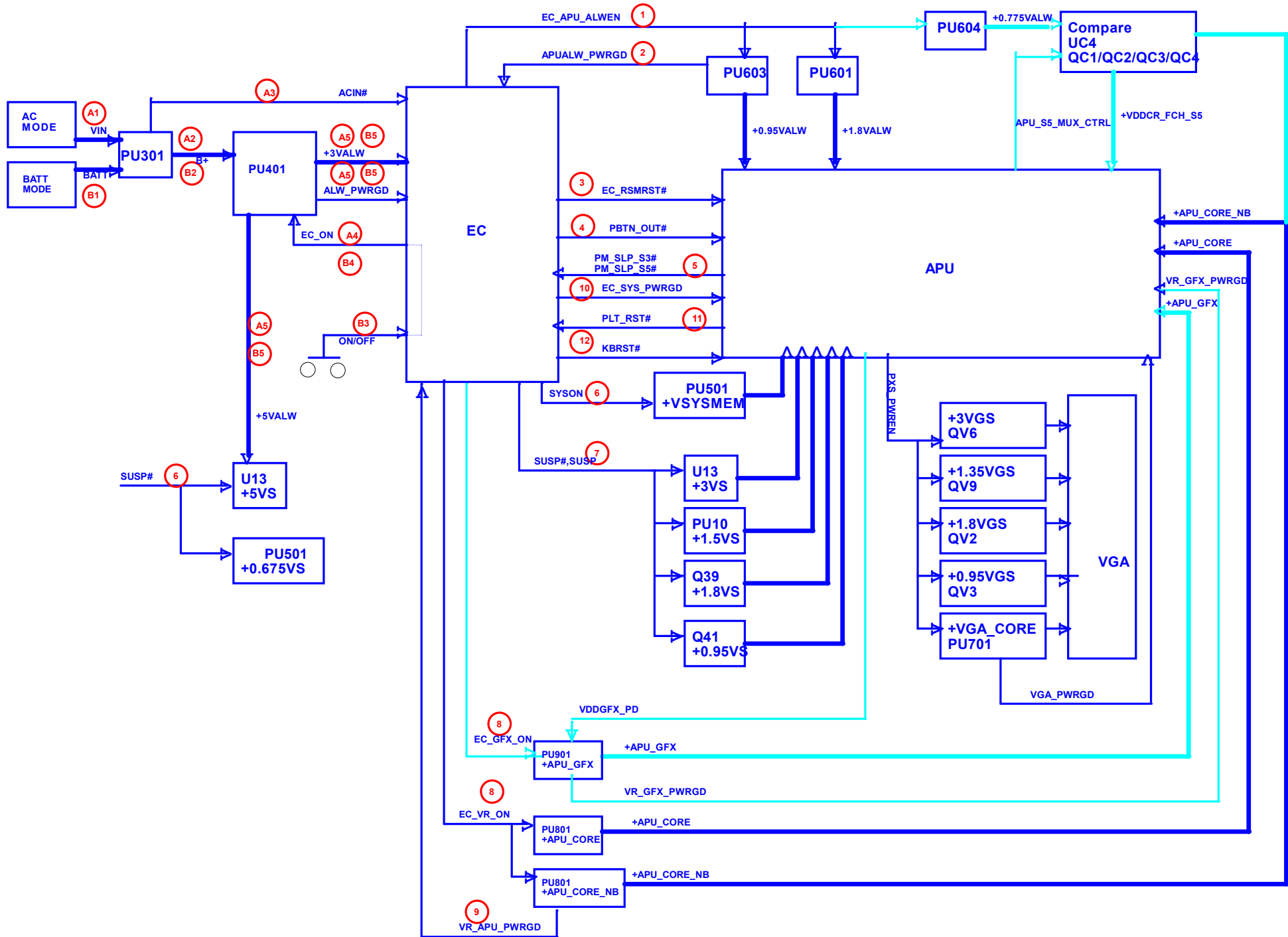



Board ID




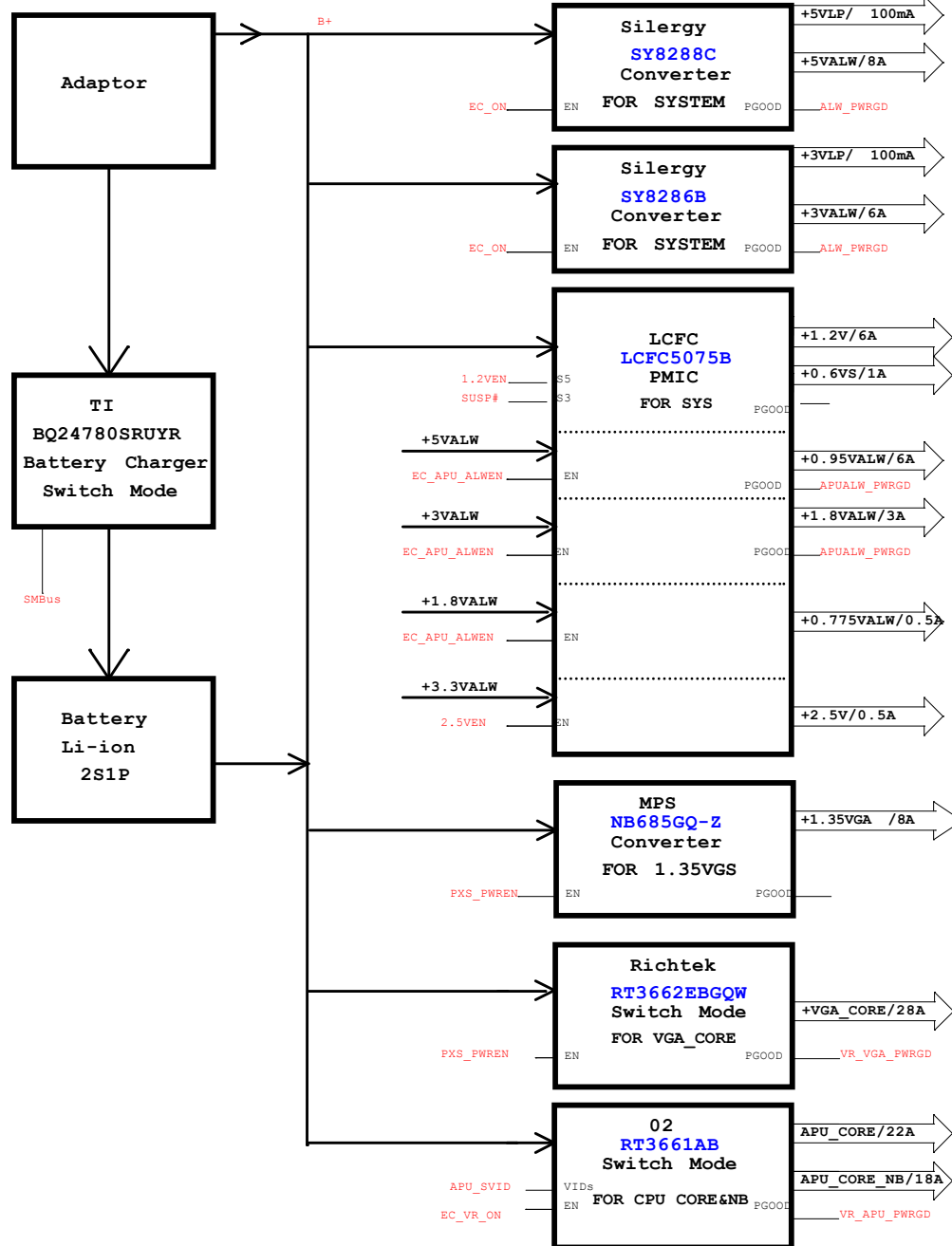
BOARD Config.	BOARD_ID0	BOARD_ID3
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15 ' '	0	1
17 ' '	1	0





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				Custom	320AST	
				Date:	Saturday, February 04, 2017	Sheet 40 of 50

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Custom	320AST	0.2	
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JDCIN1

1 2 3 4 5 6 7

GND1  
GND2  
GND3  
GND4  
GND5  
GND6

HIGHS\_PJSS0026-8B01H

ME@

APDIN

PF101

7A\_24VDC\_429007.WRML

PL101 EMC\_NS@  
HCB2012KF-121T50\_0805

PL102 EMC\_NS@  
HCB2012KF-121T50\_0805

PJ101 JUMP 43X79

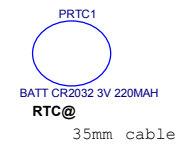
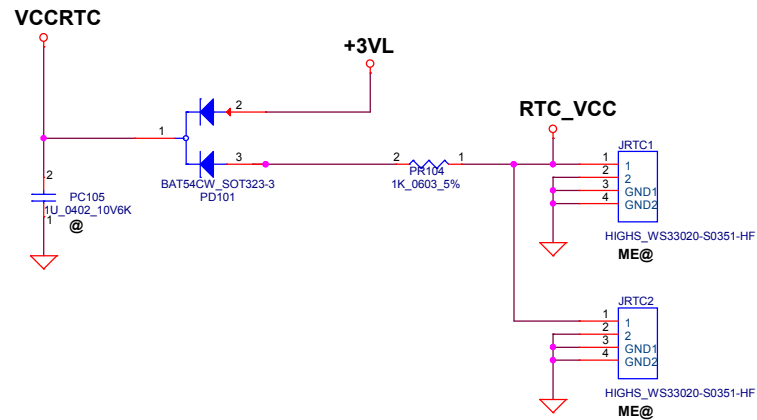
PC101 EMC@  
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PC102 EMC@  
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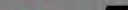
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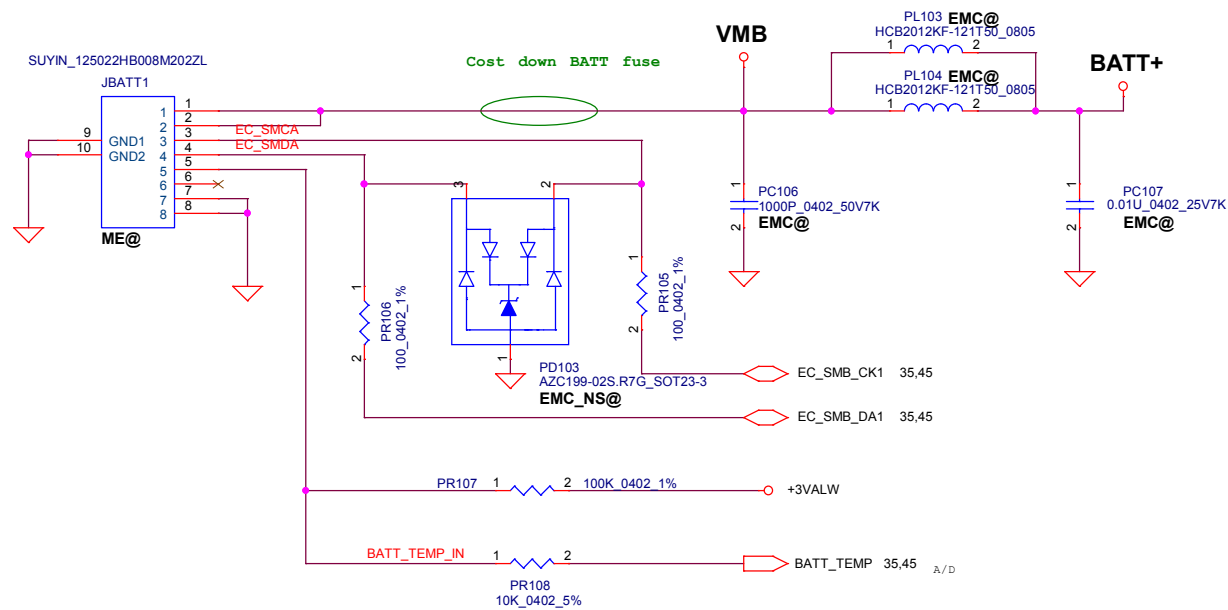
PC104 EMC@  
1000P\_0402\_50V7K

VIN



RTC Battery for GCM BOM  
(2nd source and quoted price )

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					320ABR	0.2
Date:				Saturday, February 04, 2017	Sheet 43 of 50	



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				Document Number	0.2
				Date:	320ABR
				Saturday, February 04, 2017	Sheet 44 of 50

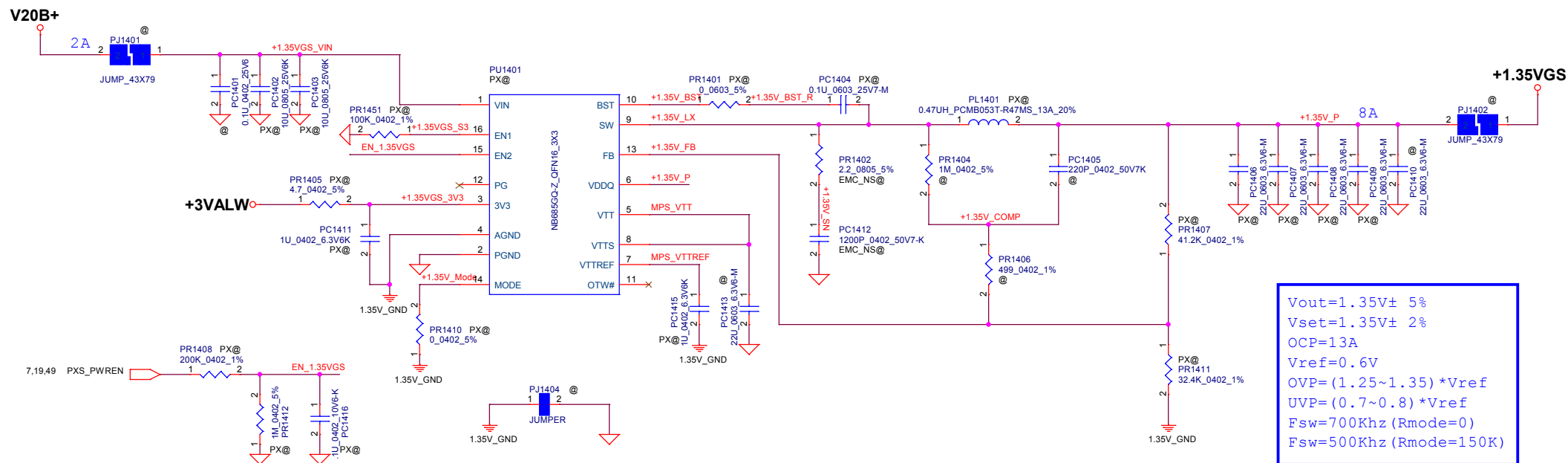








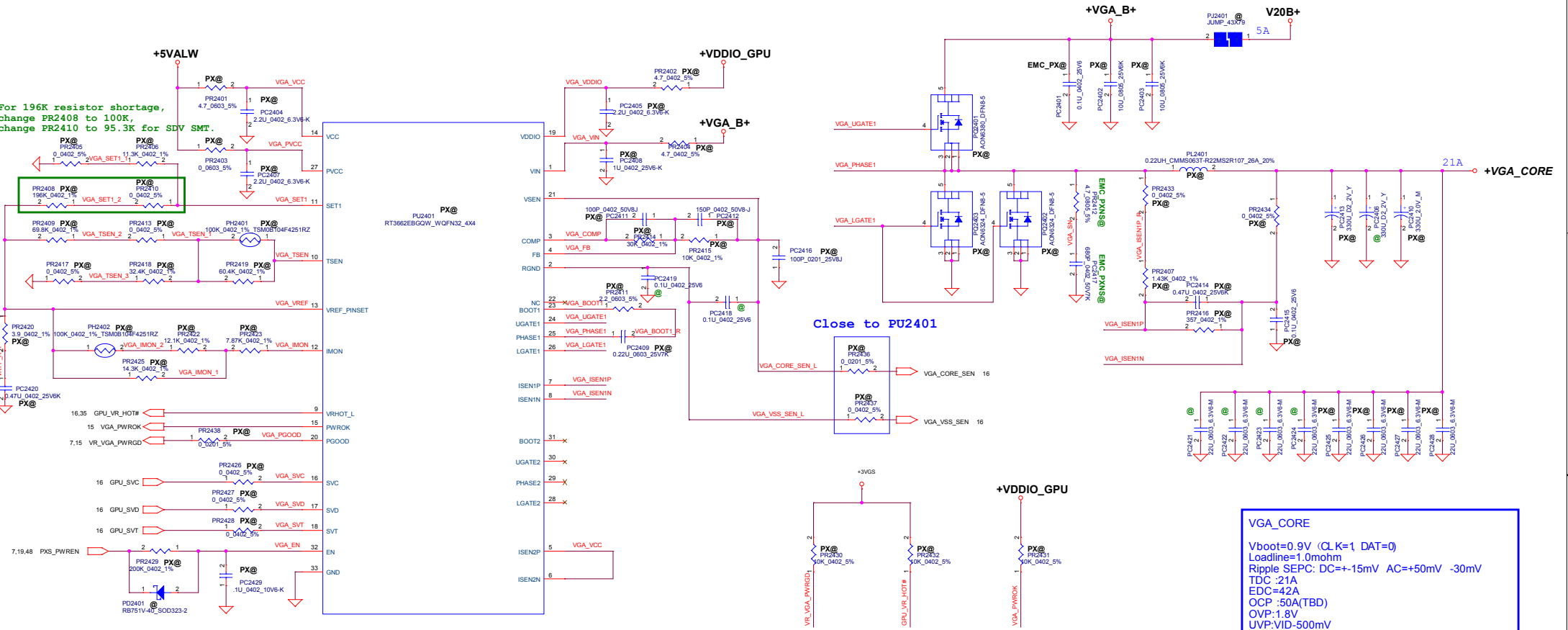




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				A3	320ABR
				Date:	Saturday, February 04, 2017
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For 196K resistor shortage,  
change PR2408 to 100K,  
change PR2410 to 95.3K for SDV SMT.



VGA\_CORE

Vboot=0.9V (CLK=1 DAT=0)  
Loadline=1.0mohm  
Ripple SEPC: DC=+-15mV AC=+50mV -30mV  
TDC :21A  
EDC=42A  
OCP=50A(TBD)  
OVP=1.8V  
UVP=VID-500mV  
FSW=400KH  
CHOKE DCR=2.1+-7% mohm

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Issued Date	2017/02/04	Deciphered Date	2017/02/04		
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				Date	Saturday, February 04, 2017
				Sheet	49 of 50

